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**Semiconductors for  
Telecommunication Applications  
Condensed Catalog**  
1987-1988

Advanced  
Micro  
Devices



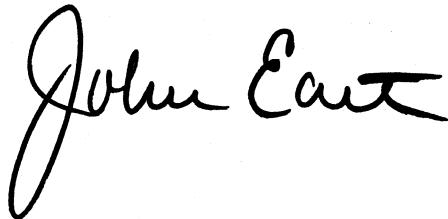


This condensed catalog is your guide to Advanced Micro Devices' communications products. These products cover a broad range of communications functions from traditional voice circuits to datacom, networking, facsimile, encryption and ISDN.

AMD's telecommunications team is committed to help you solve complex system-design problems with innovative semiconductor products. We take a systems approach in defining and designing our product. This brings together the advantages of both bipolar and MOS technologies. The benefit to you is cost-effective device partitioning. Our digital signal processing device architectures allow us to implement cost-effective system functions and still leave you the flexibility to control and/or modify device operation with software. We support your design efforts with the various hardware and software items listed in this brochure. Our worldwide network of Field Applications Engineers are always available to assist with design issues.

Complete device specifications are available from your local AMD sales office or the authorized representative listed in the back of this publication.

Sincerely,  
Advanced Micro Devices, Inc.

A handwritten signature in black ink that reads "John East". The signature is written in a cursive, flowing style with a large initial "J" and "E".

John East  
Vice President and Group Executive, Logic Group





# **Advanced Micro Devices**

## **Semiconductors for Telecommunication Applications Condensed Catalog**

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# SEMICONDUCTORS FOR TELECOMMUNICATION APPLICATIONS CONDENSED CATALOG

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# **MODEM PRODUCTS**

# A COMPLETE FSK MODEM ON ONE WORLD-CHIP™

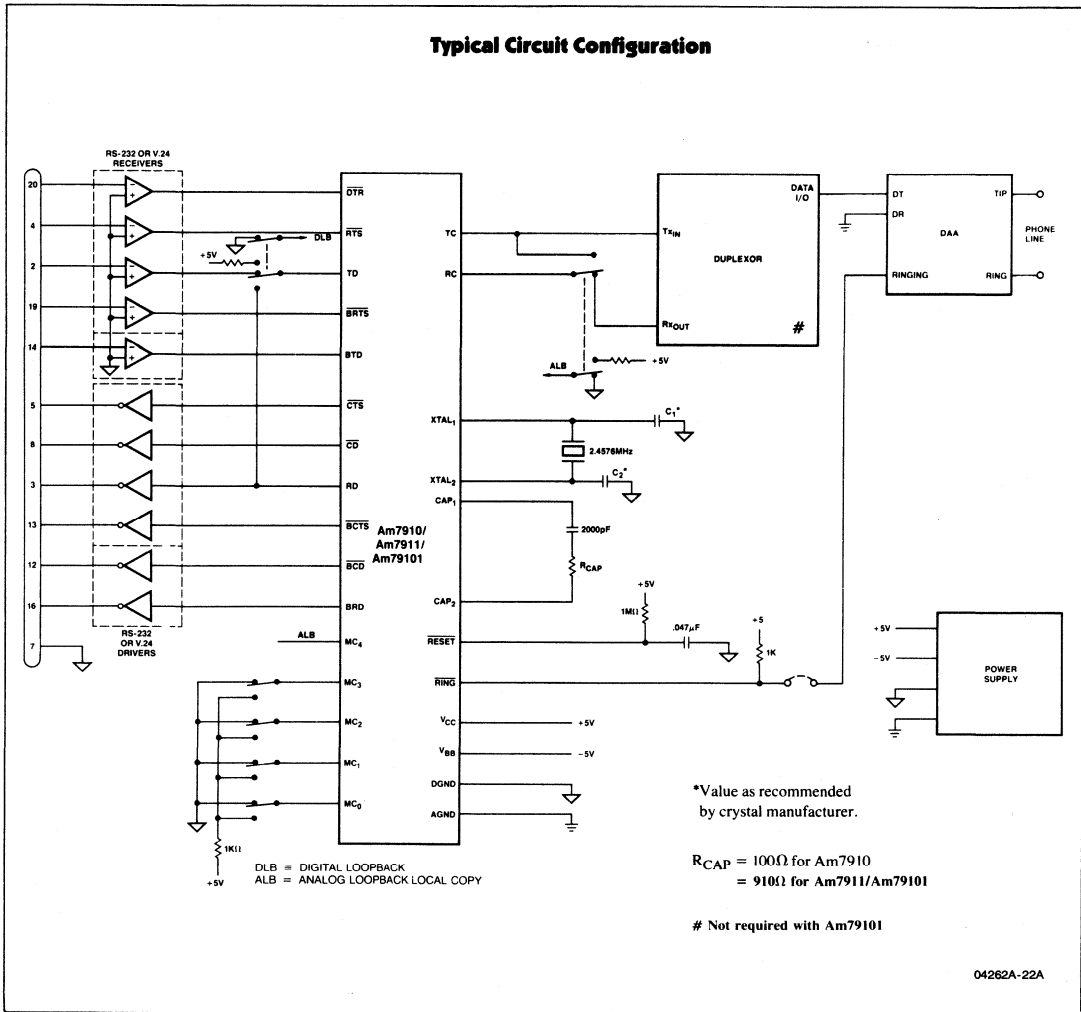
## They Are the World's First

The Am7910, Am7911 and Am79101 are the first complete, mode-programmable, asynchronous Frequency Shift Keying (FSK) modems ever offered on single LSI chips. The Am79101, Am7910 or Am7911, a crystal, and a few inexpensive, noncritical components are all you need. No external filters, no hybrids, no tuned circuits are needed, and the Am7910, Am7911 and Am79101 are programmable to any of nine world standards. Never before has the modem function been so easy to build into your products.

## They Are the World's Most Complete

All the features a modem should have are built right in. Filters are already there. So are handshake signals, auto-answer, local loopback and back channels. No extra components are required to implement these functions. In addition, the Am79101 is the only FSK modem that supports autodial with DTMF generation, Call Progress Tones Detection and Answer Tones Detection. The four-to-two-wire hybrid is also included on-chip. No FSK modem chip has ever offered so many features.

### Typical Circuit Configuration



04262A-22A

## MODEM CONFIGURATIONS

STANDARD	BIT-RATE	DUPLEX	FEATURES
Bell 103	300	Full	Originate
Bell 103	300	Full	Answer
Bell 202	1200	Half	
Bell 202	1200	Half	Line Equalizer
Bell 202*	1200	Half	150B Back Channel
Bell 202*	1200	Half	150B/Line Equalizer
CCITT V.21	300	Full	Originate
CCITT V.21	300	Full	Answer
CCITT V.23 mode 2	1200	Half	
CCITT V.23 mode 2	1200	Half	Line Equalizer
CCITT V.23 mode 2*	1200	Half	150B Back Channel
CCITT V.23 mode 2*	1200	Half	150B/Line Equalizer
CCITT V.23 mode 1	600	Half	

\*Am7911 and Am79101 only.

### Each is a **WORLD-CHIP™**

No matter where you market your product, the Am7910, the Am7911 or the Am79101 is the perfect modem solution. Without any additional circuitry, either one can be switched to any of nine Bell or CCITT standards. The flexibility of Digital Signal Processing (DSP) allows systems built with the AMD modems to be used all over the world without modification to the modem circuit.

Whether your equipment is intended for leased-line or switched-network applications, AMD has the FSK modem for you. For switched-network applications, use the Am7910 or Am79101. All of the carrier detects and handshake timings are compatible with the Bell and CCITT recommendations for switched network use. For leased-line and telex applications, use the Am7911. The Am7911 carrier detect and handshake timing is compatible with the requirements for leased-line and telex applications, including CCITT recommendation R.20.

The Am79101 provides full autodial support with on-chip DTMF generation, Call Progress Tones Detection and discrete Answerback Tones Detection.

### Selectable to Any of Nine Different World Standards

These modems are designed to be used in equipment all over the world. The devices operate in Bell 103 and 202, and CCITT V.21 and V.23 modem configuration at baud rates from 300 to 1200 bps (with back channel). 1200 bps full-duplex operation is also available using Bell 202 and CCITT V.23 loopback modes over four-wire lines. Mode selection is controlled by five simple programming inputs. No crystals need to be changed. No extra resistors, capacitors, or interface circuits are needed. Just switch a few control lines.

# Am79101

FSK Autodial Modem  
WORLD CHIP

## DISTINCTIVE CHARACTERISTICS

- Bell 103, 113, 108 and CCITT V.21 compatible at 300 bps full duplex
- Bell 202 and CCITT V.23 compatible at 1200 bps half duplex with up to 150 bps backward channel (CCITT V.23 modes with optional soft carrier turn-off feature)
- Single-chip Digital Signal Processor
- Autodial support
  - Dual-Tone Multi-Frequency (DTMF) tone generation
  - Call Progress Tones Detection
  - Answerback Tones Detection
- Integral 4- to 2-wire hybrid
- Public Switched Telephone Network (PSTN) response times
- Serial RS-232C/CCITT V.24 type handshake interface and protocol

## GENERAL DESCRIPTION

The Am79101 World Chip is a single-chip asynchronous Frequency Shift Keying (FSK) modem that is compatible with the applicable Bell and CCITT-recommended standards for 103/113/108, 202, V.21 and V.23-type modems. All modulation, demodulation, filtering, analog-to-digital and digital-to-analog functions are provided on-chip.

Using the features described below, an intelligent autodial, auto answer FSK modem may be implemented with only an Am79101 single-chip under the control of a host microprocessor and a Protective Phone Line Interface (PPLI) circuit.

The modem operates in a serial asynchronous mode, the serial interface supports the RS-232C/CCITT V.24-type handshake signals at TTL levels.

The modem analog interface provides an internal hybrid for the 4- to 2-wire conversion. Auxiliary functions performed within the Am79101 include:

Autodial support with DTMF generation and Call Progress Tones Detection.

Discrete answer tones detection (Bell and CCITT).

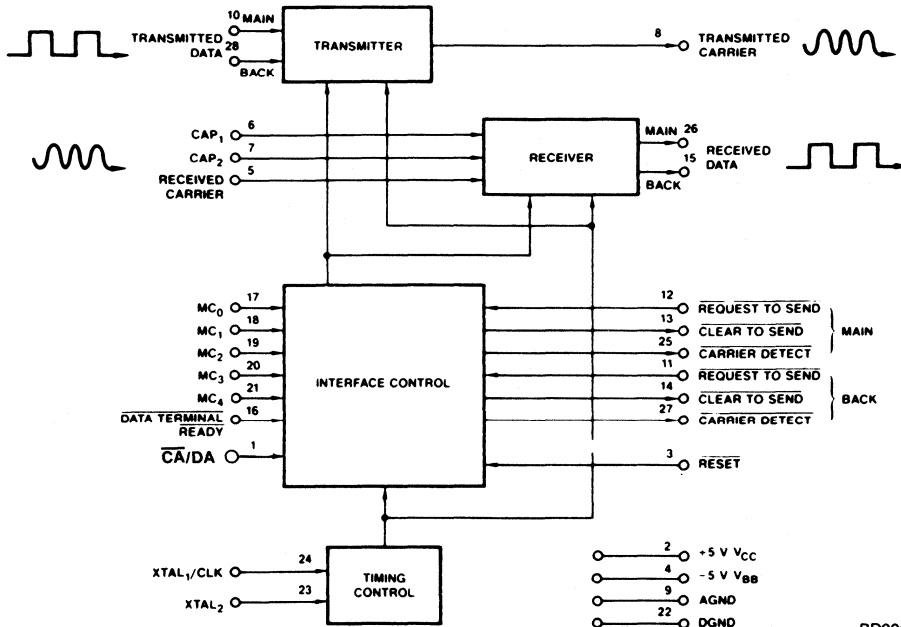
Autoanswer support.

Analog loopback support.

The Am79101 is housed in 28-pin plastic leaded chip carrier and 28-pin plastic and ceramic dual-in-line packages.

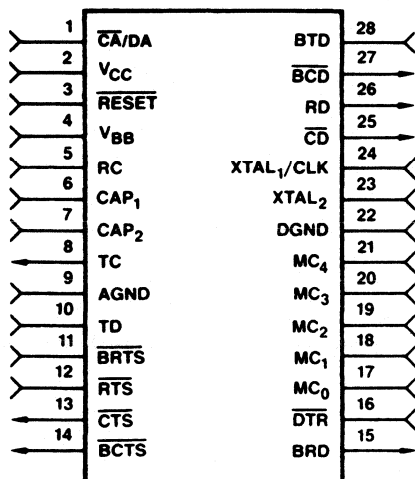
Connection to the telephone network may be via a PPLI or an acoustic coupler. All digital I/O signals are TTL-compatible (except the external clock and RESET signals) and the circuit operates from  $\pm 5$  volts.

## BLOCK DIAGRAM

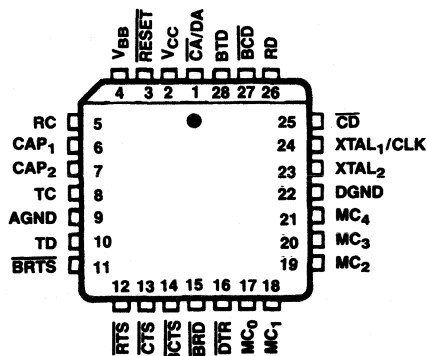


BD002791

## CONNECTION DIAGRAMS



**DIP**



**PLCC**

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following:

Device number, speed option (if applicable), package type, temperature range, and optional processing.

**AM79101**

**D**

**C**

**B**

Optional Processing  
Blank = Standard processing  
B = Burn-in

Temperature  
C = Commercial (0°C to +70°C)  
I = Industrial (-40°C to +85°C)  
E = Extended (-55°C to +125°C)

Package  
D = 28-Pin Ceramic DIP (CD 028)  
P = 28-Pin Plastic DIP (PD 028)  
J = 28-Pin PLCC (PL 028)

AMD Device Type  
FSK Modem

### Valid Combinations

AM79101	DC, DCB, DI, DIB, PC, DE, DEB, JC
---------	---

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations and to obtain additional data on AMD's standard military grade product.

# Am7910

FSK MODEM  
WORLD-CHIP™

## DISTINCTIVE CHARACTERISTICS

- Complete FSK MODEM in a 28-pin package – just add line interface
- Compatible with Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications
  - 1200 bps full duplex on 4-wire line
- All digital signal processing, digital filters, and ADC/DAC included on-chip
  - No external filtering required
- Includes essential RS-232/CCITT V.24 handshake signals
  - Dial-up network response times
- Auto-answer capability
- Local copy/test modes

## GENERAL DESCRIPTION

The Am7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. It is pin-selectable for baud rates of 300, 600 or 1200 bits per second, and is compatible with the applicable Bell and CCITT-recommended standards for 103/113/108, 202, V.21 and V.23-type modems. Five mode control lines select a desired modem configuration.

Digital signal processing techniques are employed in the Am7910 FSK Modem to perform all major functions such as modulation, demodulation, and filtering. The Am7910 contains on-chip analog-to-digital and digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT

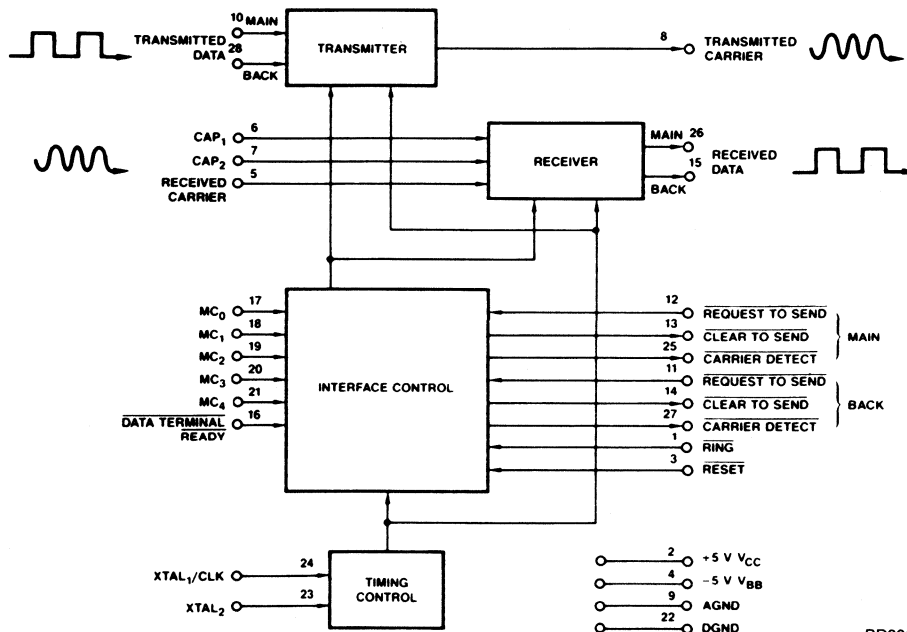
V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A Data Access Arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

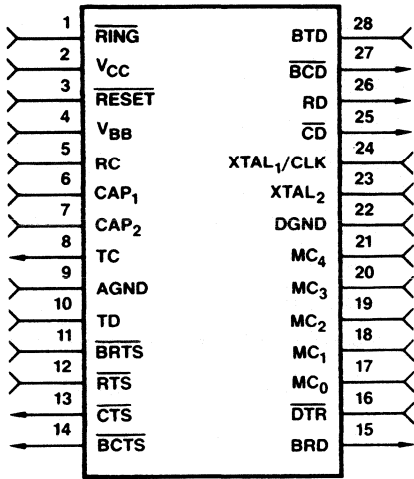
The Am7910 is fabricated using N-channel MOS technology in a 28-pin package. All the digital input and output signals (except the external clock and RESET signals) are TTL-compatible. Power supply requirements are  $\pm 5$  volts.

## BLOCK DIAGRAM

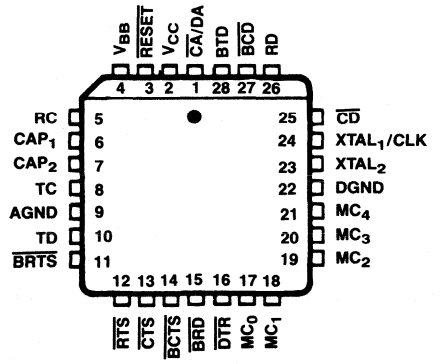


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## CONNECTION DIAGRAMS



**DIP**

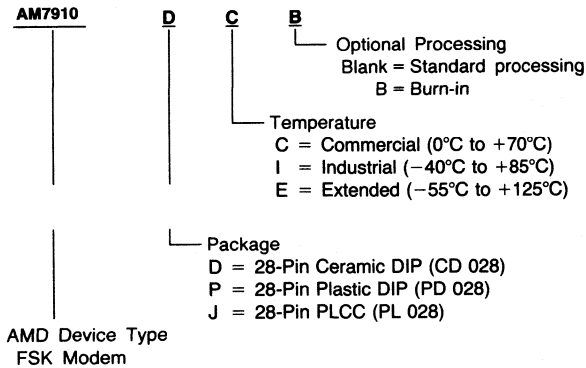


**PLCC**

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following:  
 Device number, speed option (if applicable), package type, temperature range, and optional processing.



### Valid Combinations

AM7910	DC, DCB, DI, DIB, PC, DE, DEB, JC
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### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations and to obtain additional data on AMD's standard military grade product.

# Am7911

FSK MODEM  
WORLD-CHIP™

## DISTINCTIVE CHARACTERISTICS

- Complete FSK MODEM in a 28-pin package — just add line interface
- Compatible with Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications
  - Mode-selectable 5 or 150 baud backward channel for Bell 202
  - Up to 150 baud on V.23 backward channel
  - CCITT V.23 modes with optional soft carrier turn-off feature
- 1200 bps full duplex on 4-wire line
- All digital signal processing, digital filters, and ADC/DAC included on-chip
  - No external filtering required
- Includes essential RS-232/CCITT V.24 handshake signals
  - Fast response times for leased-line networks
- Auto-answer capability
- Local copy/test modes

## GENERAL DESCRIPTION

The Am7911 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem intended for use in leased-line applications. It is pin-selectable for baud rates of 300, 600, or 1200 bits per second, and is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration; for Bell 202 applications, the Am7911 modem provides a 150 bps back channel in addition to the standard 5 bps channel, and for V.23 up to 150 bps back channel operation is possible.

Digital signal processing techniques are employed in the Am7911 modem to perform all major functions such as modulation, demodulation, and filtering. The Am7911 contains on-chip analog-to-digital and digital-to-analog

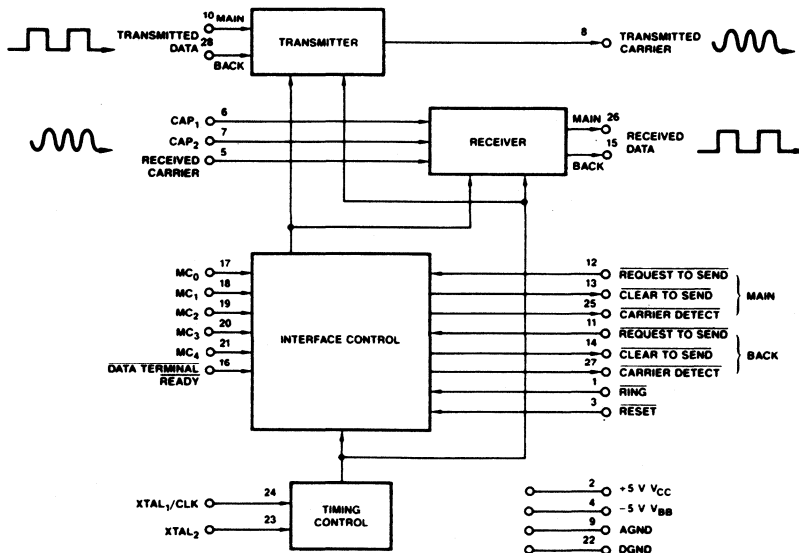
converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to the internal crystal oscillator amplifier or by applying an external clock signal.

A Data Access Arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

The Am7911 is fabricated using N-channel MOS technology in a 28-pin package. All the digital input and output signals (except the external clock and RESET signals) are TTL compatible. Power supply requirements are  $\pm 5$  volts.

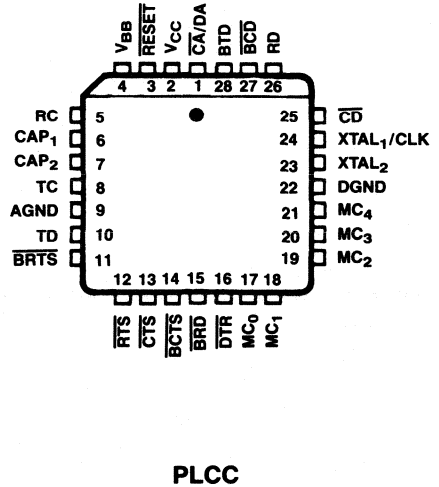
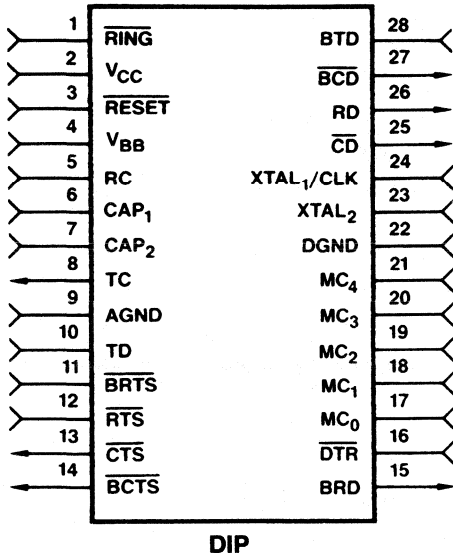
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BD002791



## CONNECTION DIAGRAMS

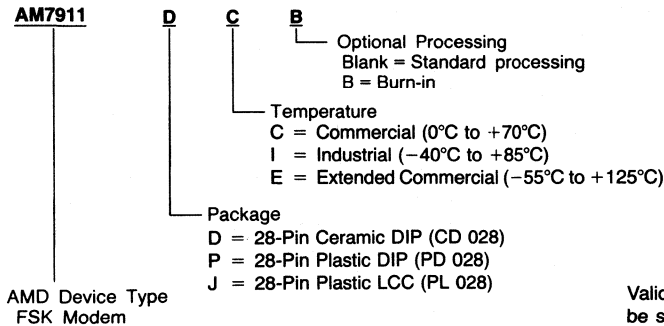


## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following:

Device number, speed option (if applicable), package type, temperature range and optional processing.



Valid Combinations	
AM7911	DC, DCB, DE, DI, DIB, PC, DE, DEB, JC

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations and to obtain additional data on AMD's standard military grade product.

# **A COMPLETE MODEM ON A SINGLE CHIP MEETS INTERNATIONAL AND NORTH AMERICAN STANDARDS**

## **Am79CV12—Full-Duplex 1200/300 bps, CCITT V.22, V.21 and Bell 212A Compatible.**

The Am79CV12 is a single-chip IC modem that incorporates and supports all of the features required in intelligent modems. Only the control and a simple protective phone line interface are required to implement a complete intelligent modem.

This microprocessor compatible datacom peripheral provides for the easy integration of the intelligent modem functions into computers, terminals, as well as stand-alone and card modems.

**Table 1. Full Duplex Modem Configurations**

<b>Standard</b>	<b>Bit Rate</b>	<b>Application</b>	<b>Mode</b>
BELL 212A	1200	North America	High Speed
BELL 103	300	North America	Low Speed
CCITT V.22	1200	International	High Speed
CCITT V.21	300	International	Low Speed

The Am79CV12 is a new member of AMD's growing family of advanced technology telecom products utilizing Digital Signal Processing (DSP) techniques. The Am79CV12 incorporates all of the handshake timings to be compatible with Bell 212A modems on the switched network. It will also fall back to 300 bps when communicating with Bell 103-type modems.

## **ARCHITECTURE**

The Am79CV12 also includes the handshake timings required for compliance with CCITT recommendations for V.22 and V.21 modems.

The Am79CV12 Dialer Modem Peripheral supports two digital data interfaces and one analog interface. The serial digital interface operates in synchronous and asynchronous modes; asynchronous parallel digital data transfer is supported with an integral UART. Digital Signal Processing is used to perform most of the major modem functions.

# Am79C12

Dialer Modem Peripheral (DMP)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- 1200/300 bps full duplex — Bell 212A compatible
  - Single-chip Digital Signal Processor
  - Coherent Differential Quaternary Phase Shift Keying/Frequency Shift Keying (DQPSK/FSK) demodulator
- Parallel Microprocessor Interface
  - Register-controlled modem operation
  - Integral UART for parallel data transfer
- Serial RS-232C type handshake interface
  - Selectable serial data transfer
- Auto-dial support
  - Dual-Tone Multi-Frequency (DTMF) tone generation
  - Pulse dial-through support
  - Call Progress tone detection
  - Answerback tone detection
- Single +5-volt CMOS technology
  - Low-power standby operation
- Integral 4- to 2-wire hybrid
  - External Analog Input

## GENERAL DESCRIPTION

The Am79C12 DMP is a single-chip 1200/300 bps full-duplex voiceband modem that operates over the switched telephone network. It is compatible with the Bell 212A (1200 bps) and Bell 103/113 (300 bps) modem specifications. All modulation, demodulation, filtering, analog-to-digital, and digital-to-analog conversion functions for both the transmitter and receiver are provided on-chip.

Using the features described below, an intelligent autocall, autoanswer modem may be implemented with only an Am79C12 single chip, under the control of a host microprocessor and a Protective Phone Line Interface (PPLI) circuit.

The Am79C12 DMP contains a standard microprocessor interface to connect directly to the host processor or controller. An on-chip UART also provides such functions as parallel data transfer, parity generation and checking, as well as overrun and framing error detections. The "break" signal is both generated and detected by circuitry inside the modem chip.

At 1200 bps the modem can operate in either bit-synchronous or character-asynchronous transmission and reception formats; 300 bps operation is always asynchronous.

The modem may be selected for parallel or serial data transmission under software control. The serial interface

supports the standard RS-232C-type handshake signals. The modem analog interface provides both an internal hybrid and an external analog input to allow phone-line access for a telephone handset or another modem.

Auxiliary functions performed within the Am79C12 include:

- Modem training
- Remote-modem speed indication
- Autocalling support, DTMF generation, and Call Progress Tone Detection (CPTD)
- Autoanswer support
- Parallel control of serial and parallel data interfaces
- Remote digital loopback support
- Analog-loopback support

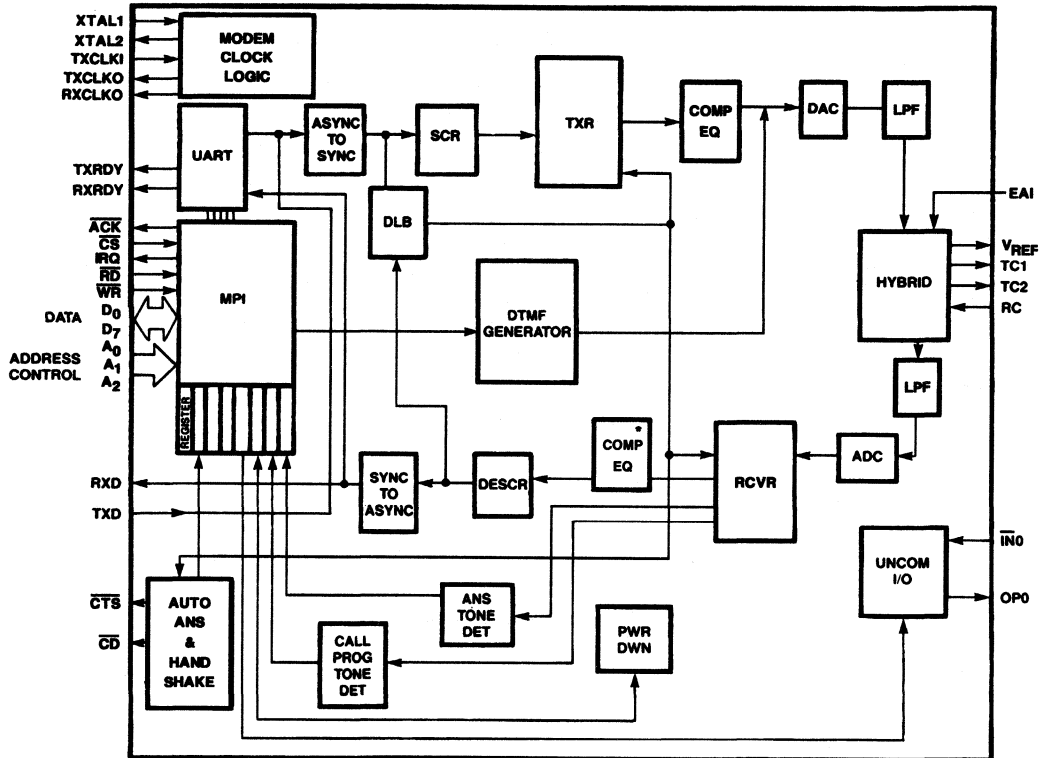
One interrupt input and one programmable output are provided on-chip for controlling user-definable functions such as ON/OFF-HOOK, analog loopback, and ring detection from a PPLI.

The modem utilizes CMOS technology and is housed in 44-pin plastic leaded chip carrier and 40-pin plastic dual-in-line packages. All signal processing is performed digitally to ensure high stability and reproducibility over a comprehensive set of transmission test conditions (see block diagram on following page for functional blocks of the Am79C12).

Connection to the telephone network may be via a PPLI or an acoustic coupler. All digital I/O signals are TTL-compatible and the circuit operates from a single +5-volt supply.

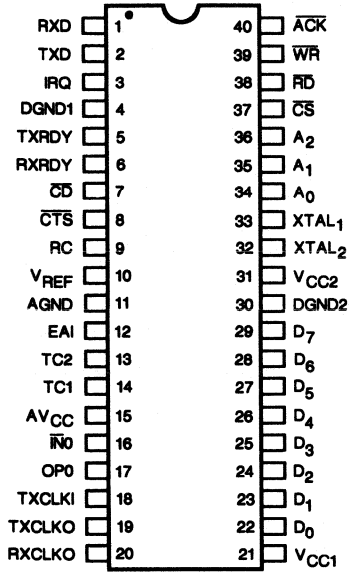
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Am79C12

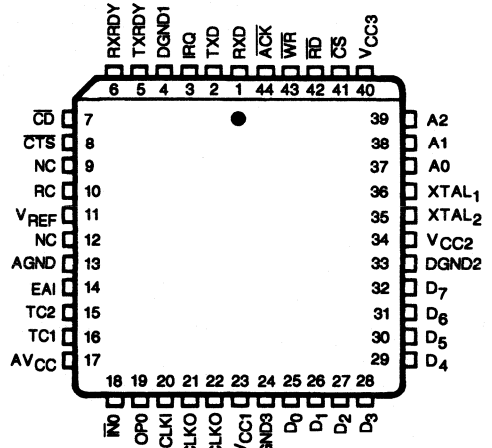


BD005722

## CONNECTION DIAGRAMS



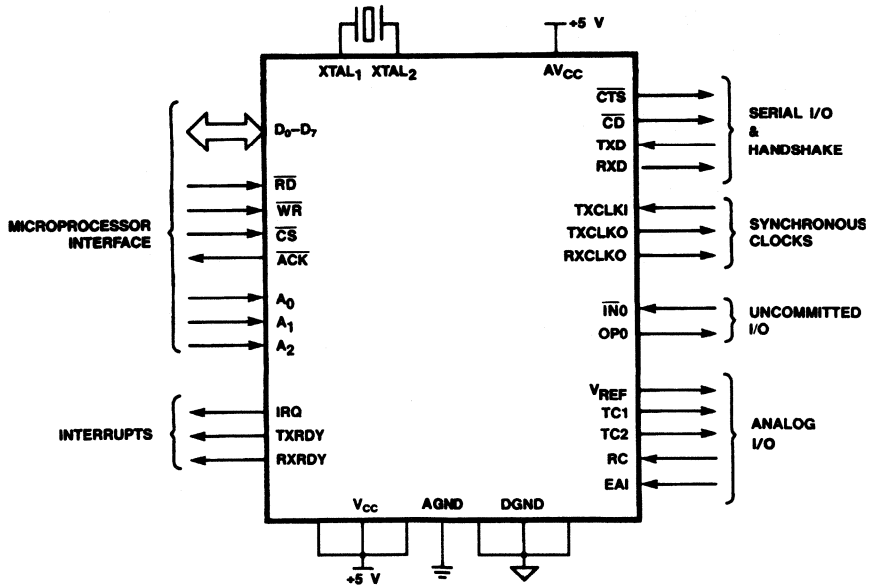
CD009850



CD009840

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



LS002031

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing

AM79C12

P

C

B

**e. OPTIONAL PROCESSING**

Blank = Standard processing  
B = Burn-in

**d. TEMPERATURE RANGE**

C = Commercial (0 to +70°C)  
I = Industrial (-40°C to +85°C)

**c. PACKAGE TYPE**

P = 40-Pin Plastic DIP (PD 040)  
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

**b. SPEED OPTION**

Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**

Am79C12  
Dialer Modem Peripheral

Valid Combinations	
AM79C12	PC, PCB, JC, JCB

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am79CV12

Dialer Modem Peripheral (DMP)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- 1200/300 bps full-duplex—Bell 212A, V.22, and V.21 compatible
  - Single-chip Digital Signal Processor
  - Coherent Differential Quaternary Phase Shift Keying/ Frequency Shift Keying (DQPSK/FSK) demodulator
- Parallel Microprocessor Interface
  - Register-controlled modem operation
  - Integral UART for parallel data transfer
- Serial RS-232C/V.24 type handshake interface
  - Selectable serial data transfer
- Autodial support
  - Calling tone generation
  - Dual-Tone Multi-Frequency (DTMF) tone generation
  - Pulse dial-through support
  - Call Progress tones detection
  - Programmable Answerback tones detection
- Single +5-volt CMOS technology
  - Low-power standby operation
- Integral 4- to 2-wire hybrid
  - External Analog Input

## GENERAL DESCRIPTION

The Am79CV12 DMP is a single-chip 1200/300 bps full-duplex voiceband modem that operates over the switched telephone network. It is compatible with the Bell 212 and V.22 sequences (1200 bps), as well as the Bell 103/113 and V.21 sequences (300 bps). All modulation, demodulation, filtering, analog-to-digital, and digital-to-analog conversion functions for both the transmitter and receiver are provided on-chip.

Using the features described below, an intelligent autocal, autoanswer modem may be implemented with only an Am79CV12 single-chip, under the control of a host microprocessor and a Protective Phone Line Interface (PPLI) circuit.

The Am79CV12 DMP contains a standard microprocessor interface to connect directly to the host processor or controller. An on-chip UART also provides such functions as parallel data transfer, parity generation and checking, as well as overrun and framing error detections. The "break" signal is both generated and detected by circuitry inside the modem chip.

At 1200 bps the modem can operate in either bit-synchronous or character-asynchronous transmission and reception formats; 300 bps operation is always asynchronous.

The modem may be selected for parallel or serial data transmission under software control. The serial interface supports the standard RS-232C/V.24-type handshake signals. The modem analog interface provides both an internal hybrid and an external analog input to allow phone-line access for a telephone handset or another modem.

Auxiliary functions performed within the Am79CV12 include:

- 1300 Hz calling tone; 550 or 1800 Hz guard tones
- Programmable Answerback tones detection
- Modem training
- Remote-modem speed indication
- Autocalling support, DTMF generation, and Call Progress Tones Detection (CPTD)
- Autoanswer support
- Parallel control of serial and parallel data interfaces
- Remote digital loopback support
- Analog-loopback support

One interrupt input and one programmable output are provided on-chip for controlling user-definable functions such as ON/OFF-HOOK, analog loopback, and ring detection from a PPLI.

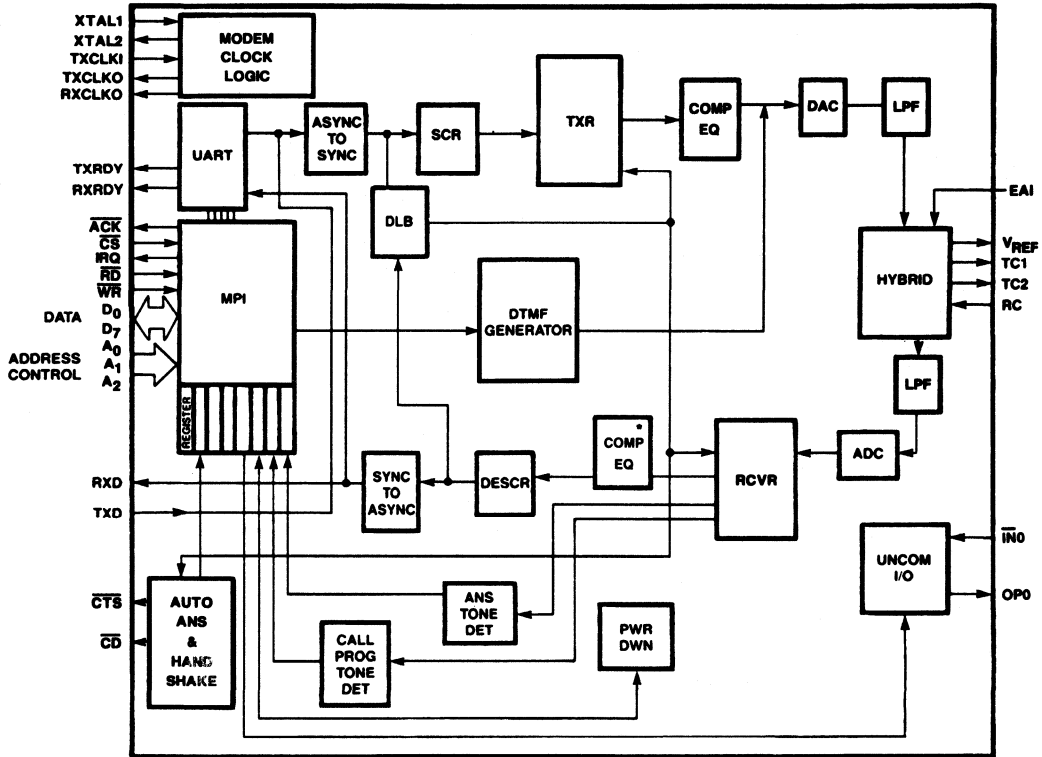
The modem utilizes CMOS technology and is housed in 44-pin plastic leaded chip carrier and 40-pin plastic dual-in-line packages. All signal processing is performed digitally to ensure high stability and reproducibility over a comprehensive set of transmission test conditions (see block diagram on following page for functional blocks of the Am79CV12).

Connection to the telephone network may be via a PPLI or an acoustic coupler. All digital I/O signals are TTL-compatible and the circuit operates from a single +5-volt supply.

The Am79CV12 supersedes and is both pin and functionally compatible with the Am79C12.

# BLOCK DIAGRAM

## Am79CV12

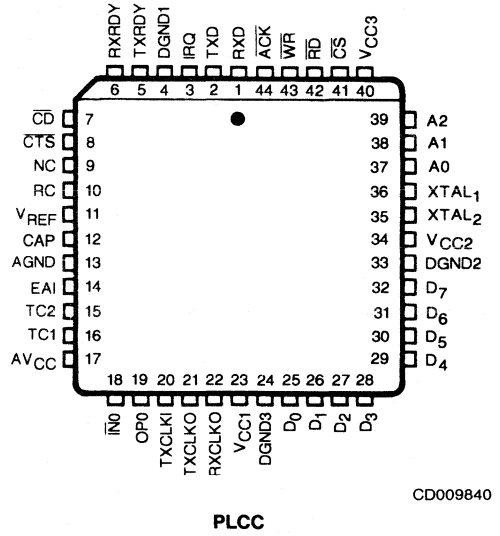
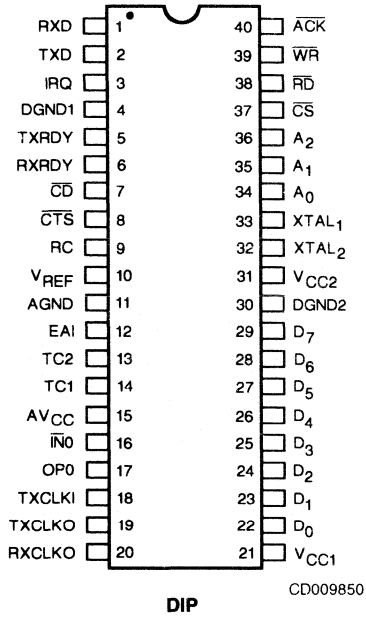


BD005722

\*Applies to PLCC package only.

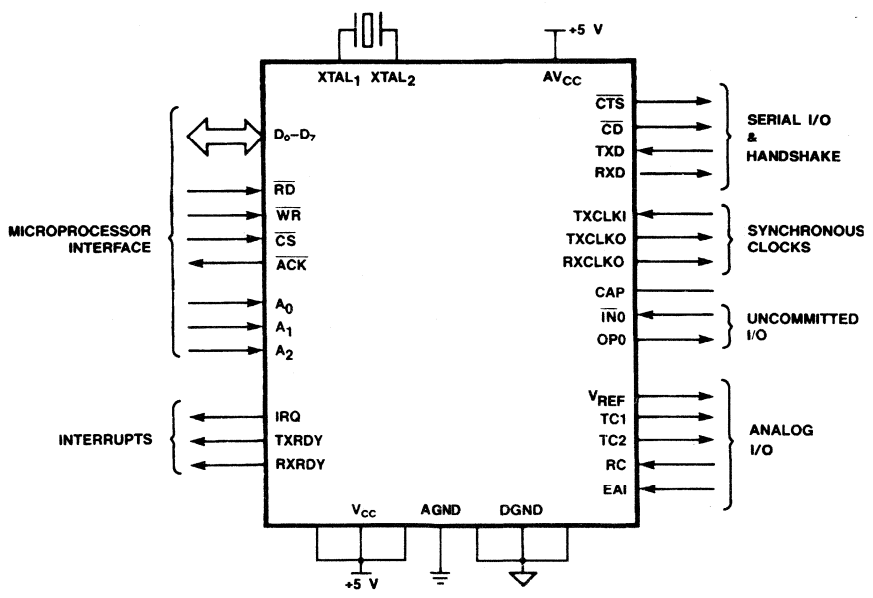


## CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM79CV12

P

C

B

e. **OPTIONAL PROCESSING**  
 Blank = Standard processing  
 B = Burn-in

d. **TEMPERATURE RANGE**  
 C = Commercial (0 to +70°C)  
 I = Industrial (-40°C to +85°C)

c. **PACKAGE TYPE**  
 P = 40-Pin Plastic DIP (PD 040)  
 J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

b. **SPEED OPTION**  
 Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**  
 Am79CV12  
 Dialer Modem Peripheral

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM79CV12	PC, PCB, JC, JCB

# Am7913/Am79C13

'AT' Modem Controller (ATMC)

## ADVANCE INFORMATION

### DISTINCTIVE CHARACTERISTICS

- Controls Am79C12 and Am79CV12 Full-Duplex 1200/300 bps Modems
- Interprets Hayes® 'AT' Command Set
- Compatible with 8250/16450 PC-based UARTs
- Automatic Character Synchronization
  - Baud rate determination
  - Character format determination
- Automatic Answer Function
  - Adapts to originating modem's baud rate
- Automatic Dialing Function
  - DTMF dialing
  - Pulse dialing
  - Special PBX features
- Extensive Modem Testing
  - Analog Loopback
  - Digital Loopback
  - Remote Digital Loopback
- Dialtone and Busy Signal detection
- Command Line Repeat Capability
- Software Control of Speaker Volume
- Voice/Data Switching
- Programmable Product ID
- Supports External EPROM for User-Custom Code Additions
- Available in:
  - Low-cost NMOS as Am7913
  - Low-power CMOS as Am79C13
- TTL Compatible I/O with Single +5-volt Supply
- Available in Plastic Leaded Chip Carrier or Plastic DIP Packaging

### GENERAL DESCRIPTION

The Am7913/Am79C13 'AT' Modem Controller (ATMC) is designed to interpret the Hayes® 'AT' Command Set and in turn control the Am79C12/79CV12 Full-Duplex 1200/300 bps Modem in a PC Plug-in or Box Modem environment. With the addition of the 8250 UART for PC- and XT-compatible computers, or the 16450 UART for AT-compatible computers, the Am7913/Am79C13 runs with industry-standard software packages to emulate a "Smart Modem." RS-232C Transceivers replace the UART for Box Modem applications.

In the Command Mode, the Am7913/Am79C13 communicates with industry-standard application software via its serial port, and configures the Am79C12/79CV12 Modem via its parallel port. With the reception of the 'AT' Command Line Start Characters, the Am7913/Am79C13 automatically determines the application software's baud rate (1200/300) and character format including the number of data and stop bits and type of parity used. In the Data Mode, the Am7913/Am79C13 monitors the data being passed to the Am79C12/79CV12 Modem, waiting for a programmable Escape Sequence which the application software uses to return the Am7913/Am79C13 back to the Command Mode for parameter changes.

The intelligent dialing and answering features greatly expand the versatility of the Am7913/Am79C13. Automatic

dialing functions include programmable options for PBX applications and the intelligence to detect the presence or absence of dialtone, as well as busy signal and no answer conditions. Automatic answer functions allow the unattended modem to answer a call and automatically adapt to the originating modem's baud rate.

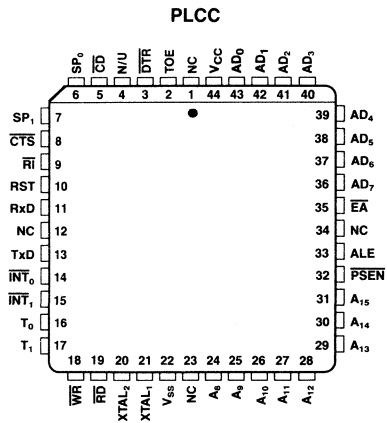
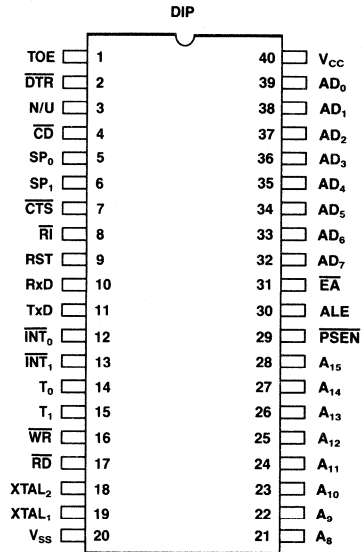
Many diagnostic features are also included for troubleshooting. These include an internal ROM checksum test to verify operation of the Am7913/Am79C13, an Analog Loopback test to verify operation of the Am79C12/79CV12 Modem, a Digital Loopback test to verify the integrity of the telephone line and remote modem, and an intelligent Remote Digital Loopback test which utilizes a special handshake with an equally sophisticated remote modem. This test can be initiated by either modem to verify the telephone line's operation with the opposite modem.

Speaker control is included to allow "hands free" feedback of the modem tones on the telephone line. Via software, the user can control when the speaker is operating, and can select one of three speaker volumes. Optionally the user can switch the modem from data to voice communication without disconnecting and redialing the line.

®Registered trademark of Hayes Microcomputer Products.

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

## CONNECTION DIAGRAMS



# **INTEGRATED SERVICES DIGITAL NETWORK PRODUCTS**

## INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

The seven ICs on the following pages provide the bases for building terminal equipment and digital Private Automatic Branch Exchanges (PABXs) compatible with the Consultative Committee for International Telegraph and Telephone (CCITT) recommendations for the Integrated Services Digital Network (ISDN). The chip set consists of five CMOS devices used to communicate over the CCITT-recommended 'S' interface, and two bipolar ICs to handle the power requirements on the 'S' and 'U' interfaces. The devices are:

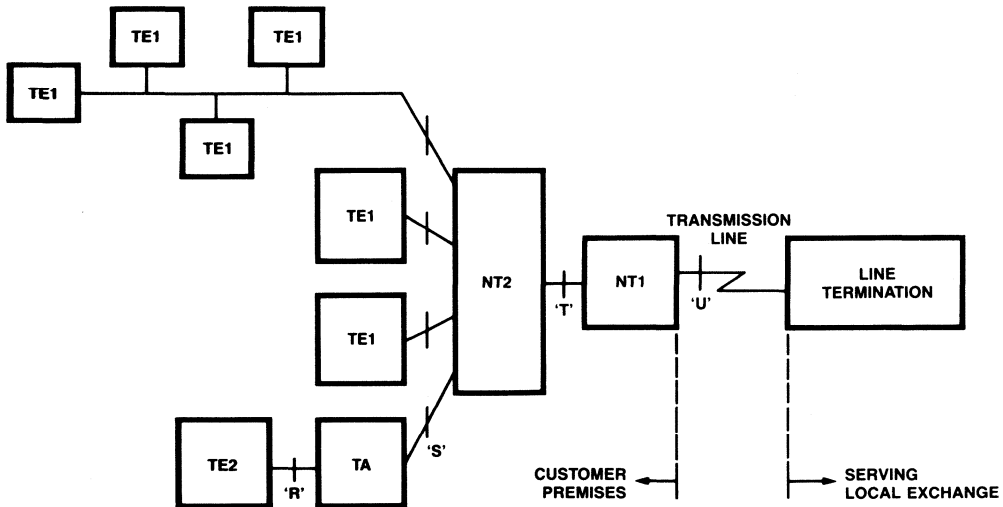
- Am79C30 Digital Subscriber Controller (DSC)
- Am79C32 ISDN Data Controller (IDC)
- Am79C31A Digital Exchange Controller (DEC)
- Am79C312 Digital Transceiver Controller (DTC)
- Am7936 Subscriber Power Controller (SPC)
- Am7938 Quad Exchange Power Controller (QEPC)

The ISDN presents to its users standard interfaces and access procedures for a wide range of digital communication, including voice, computer data, and video data. The standard interface at the basic access level allows a small set of integrated circuits to meet the requirements for a wide range of users. The subscriber interface, in CCITT terminology, is at reference point 'S'. At this inter-

face, the I-Series recommendations specify the physical, electrical, and protocol characteristics.

There are two main subscriber installations: point-to-point and point-to-multipoint, as defined by the CCITT recommendations. The ISDN Terminal Equipment (TE) behaves the same in both configurations, but the Network Terminating (NT) equipment may be different. The NTs may be located at the subscribers' premises. In larger installations, the NT may be a PABX with multiple TEs. In smaller installations a single TE may be connected to an NT.

The figure below identifies the different reference points and components of an installation. A subscriber attaches equipment to the network at reference points 'S' and 'T'. At these reference points, appropriate I-Series recommendations specify the interface requirements. The NT1 connects to the transmission line on one side, and presents the standard interface at 'T' on the other side. The NT2 is optional and connects multiple lines to one line. Terminals which operate using existing standards (e.g., RS232C) attach at reference point 'R' and a Terminal Adaptor (TA) is used for interface translation/adaption.



**CCITT ISDN Reference Points**

The four-wire 'S' interface operates at a 192 kbps bit rate comprised of:

a) a 64 kbps voice/data B1-channel; b) a 64 kbps voice/data B2-channel; c) a 16 kbps control/data D-channel; and d) a 48 kbps frame and maintenance channel.

The B1 and B2 are voice or data channels, while the D-channel is used for control or data. The information on the D-channel control packet follows the LAPD protocol defined in the CCITT recommendation. The 'S' interface frame structure contains 48 bits with a period of 250 microseconds. The frame is transmitted as a Pseudo-Ternary code containing framing, DC balancing, and contention resolution (D echo bit 'E') for point-to-multipoint applications.

The Am79C30 and Am79C32 interface at the 'S' reference point, and reside in the TE1. The Am79C30 contains the codec-filter functions for telephony, while the pin-compatible Am79C32 is only for data terminal applications. The Am79C401 IDPC interfaces with the serial port of the Am79C30 or Am79C32, and supports bit-oriented protocols for the B-channel.

The Am79C31 DEC terminates one 'S' interface on the PABX line card and provides the standard dual PCM highway to the system's backplane. The Am79C312 DTC is an optimized version of the Am79C312 for line cards using central D-channel handling.

The Am7936 provides a stable regulated 5V DC supply for ICs in the TE1, or a regulated DC voltage for ICs in the NT or power to the 'S' interface. The Am7938 QEPC supplies a regulated 40V power source for four digital telephone lines.

# Am79C30

Digital Subscriber Controller (DSC)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Terminal Equipment access to the Integrated Services Digital Network (ISDN)
  - Compatible with CCITT I-series Recommendations at the 'S' Reference Point
  - Handles both Voice and Data for Public and Private Networks
- Microprocessor, Interrupt Driven, Parallel Interface
- Full-Duplex, 3-Channel, Serial Interface
- 'S' Interface Transceiver
  - Full-Duplex, 4-Wire Operation
  - Supports Standard Bus and Short/Extended Passive Bus Arrangements
  - 192 Kbps Transfer Rate:
    - 64 Kbps voice/data B1-channel
    - 64 Kbps voice/data B2-channel
    - 16 Kbps control/data D-channel
    - 48 Kbps framing and maintenance
  - Level 1 physical layer controller
- D-Channel Processing Capability
  - Flag Insertion/Deletion
  - CRC Generation/Checking
  - Zero Insertion/Deletion
  - Incoming Address Decoders
  - Random Number Generation
- Audio Processing Capability
  - Dual Audio Inputs
  - Earpiece Output Driver
  - Loudspeaker Output Driver
  - Codec with A-Law/U-Law selection
  - Programmable DSP Equalization and Gain/Attenuation Filters
  - Programmable Sidetone Gain
  - Programmable DTMF Tone, Single Tone, and Ringer Tone Generators
- Resolution for Multiple Terminal ISDN Access Contention
- Test/Maintenance Loopbacks
- CMOS Technology with Single +5 Volt Supply, TTL Compatible

## GENERAL DESCRIPTION

The Am79C30 Digital Subscriber Controller (DSC) provides digital customer access to the ISDN. The Am79C30 is compatible with the CCITT I-series recommendations at the 'S' reference point, allowing the user of the device to design TEs that conform to international ISDN standards.

The Am79C30 provides a 192 kbps duplex digital path between the TE located in the subscriber's premises and the NT or PABX line card over 4-wires. The Am79C30 separates the bit-stream into the B1- (64 kbps), B2- (64 kbps) and D- (16 kbps) channels. The B-channels are routed to different sections of the Am79C30 under user control. The D-channel is partially processed in the Am79C30 and passed to the microprocessor for further processing.

The transmission rate of 192 kbps provides a 48-bit frame each 250 $\mu$ s for framing and maintenance. Its frame structure provides for frame synchronization and multiple terminal contention resolution, as described in the CCITT I-series recommendations. Point-to-point and point-to-multipoint connections are supported to meet both PABX and central office switching applications.

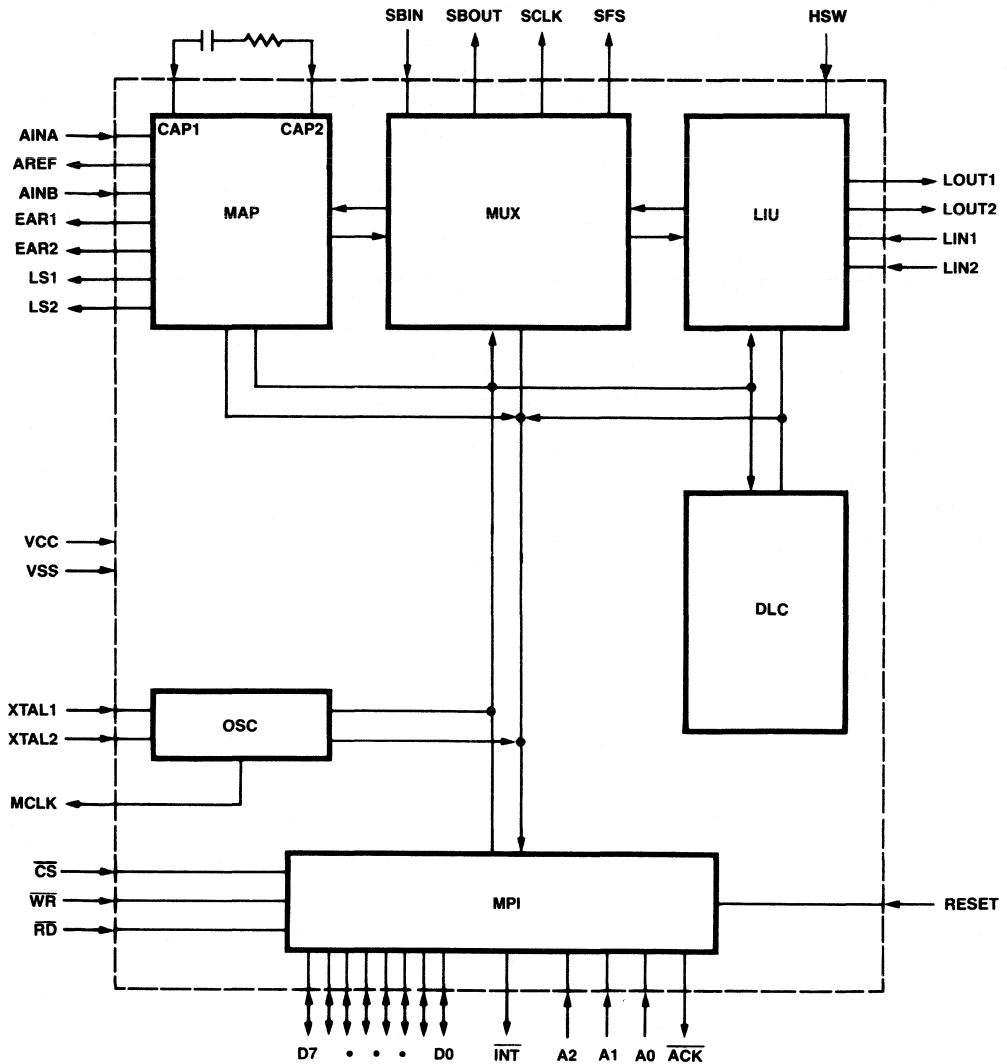
The Am79C30 can be used in two basic applications; as a voice telephone, a digital data terminal, or a voice and data terminal.

The audio processor in the Am79C30 uses Digital Signal Processing (DSP) to implement the codec and filter functions. The audio processor interfaces to a speaker, an earpiece, and two separate audio inputs. In the receive and transmit paths the user may program gain or alter the frequency response.

A serial port gives the user access to the B-channels of the Am79C30 multiplexer. This serial port may be used by data terminals and, with additional circuitry, provides access to the CCITT 'R' reference point.

The Am79C30 is controlled via a parallel interrupt-driven microprocessor interface by an external microprocessor. Using this interface, the microprocessor processes the D-channel information and programs the Am79C30 accordingly. This includes programming a multiplexer within the Am79C30 to route the B-channels as specified by the D-channel control information. The microprocessor can interrogate and program the Am79C30 via its mode, status, and error registers.

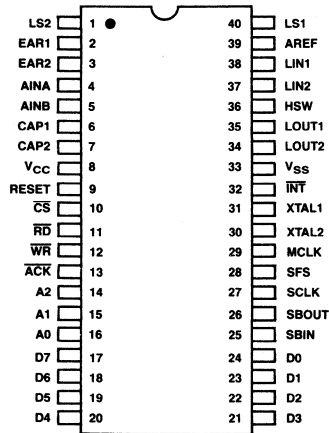
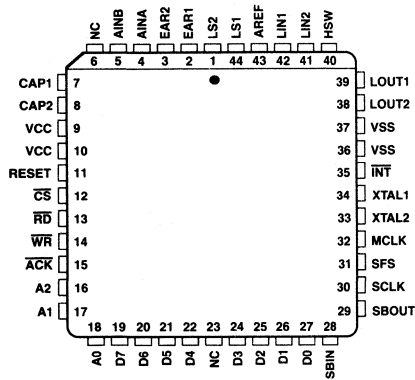




**Am79C30 DSC Block Diagram**

- MAP = Main Audio Processor
- MUX = Multiplexer
- LIU = Line Interface Unit
- OSC = Oscillator and Timing Circuitry
- MPI = Microprocessor Interface
- DLC = Data Link Controller

## CONNECTION DIAGRAMS



Note Pin 1 is marked for orientation.

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM79C30

P

C

B

- e. **OPTIONAL PROCESSING**  
Blank = Standard processing  
B = Burn-in
- d. **TEMPERATURE RANGE**  
C = Commercial (0 to +70°C)

- c. **PACKAGE TYPE**  
P = 40-Pin Plastic DIP (PD 040)  
D = 40-Pin Ceramic DIP (CD 040)  
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

- b. **SPEED OPTION**  
Not Applicable

- a. **DEVICE NUMBER /DESCRIPTION**  
Am79C30  
Digital Subscriber Controller

Valid Combinations	
AM79C30	DC, DCB, PC, PCB, JC, JCB

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am79C32

ISDN Data Controller (IDC)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Terminal Equipment access to the Integrated Services Digital Network (ISDN)
  - Compatible with CCITT I-series Recommendations at the 'S' Reference Point
  - Handles both Voice and Data For Public and Private Networks
- Microprocessor, Interrupt Driven, Parallel Interface
- Full-Duplex, 3-Channel, Serial Interface
- 'S' Interface Transceiver
  - Full-Duplex, 4-Wire Operation
  - Supports Standard Bus and Short/Extended Passive Bus Arrangements
  - 192 Kbps Transfer Rate:
    - 64 Kbps voice/data B1-channel
    - 64 Kbps voice/data B2-channel
    - 16 Kbps control/data D-channel
    - 48 Kbps framing and maintenance
- D-Channel Processing Capability
  - Level 1 physical layer controller
  - Flag Insertion/Deletion
  - CRC Generation/Checking
  - Zero Insertion/Deletion
  - Incoming Address Decoders
  - Random Number Generation
- Resolution for Multiple Terminal ISDN Access Contention
- Test/Maintenance Loopbacks
- CMOS Technology with Single +5 Volt Supply, TTL Compatible

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## GENERAL DESCRIPTION

The Am79C32 ISDN Data Controller (IDC) provides terminal equipment access to the ISDN. The Am79C32 is compatible with the CCITT I-Series recommendations at the 'S' reference point, allowing the user of the device to design TEs that conform to international ISDN standards.

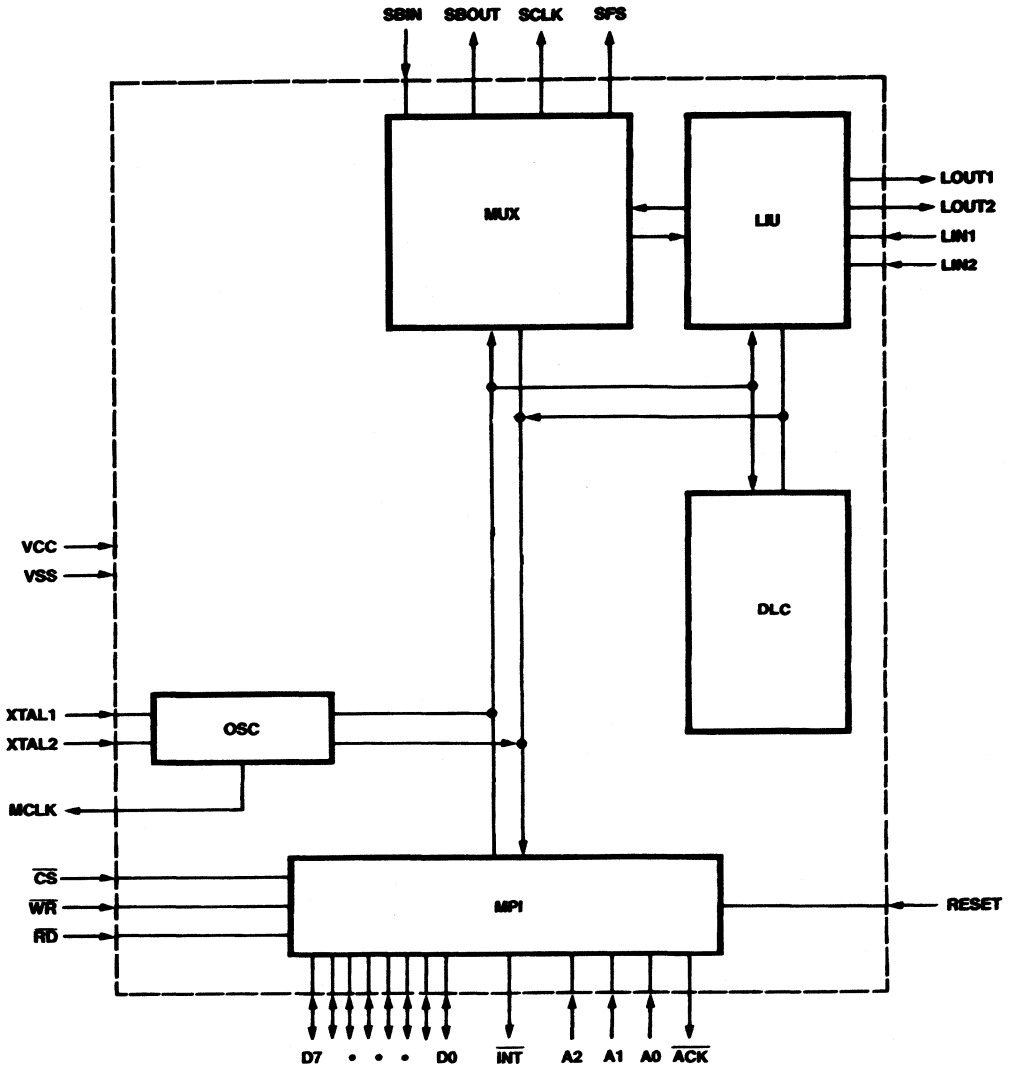
The Am79C32 provides a 192 kbps duplex digital path between the TE located in the subscriber's premises and the NT or PABX line card over 4-wires. The Am79C32 separates the bit-stream into the B1 (64 kbps), B2 (64 kbps) and D (16 kbps) channels. The B-channels are routed to different sections of the Am79C32 under user control. The D-channel is partially processed in the Am79C32 and passed to the microprocessor for further processing.

The transmission rate of 192 kbps provides a 48-bit frame each 250 $\mu$ s for framing and maintenance. Its frame structure provides for frame synchronization and multiple terminal contention resolution, as described in the CCITT I-Series recommendations. Point-to-point and point-to-multipoint connections are supported to meet both PABX and central office switching applications.

The Am79C32 is designed to be used as a digital data terminal. This device is pin for pin compatible with the Am79C30. Its internal structure is identical except the codec filter function (the main Audio Processor) has been removed. The pins relating to the main Audio Processor on the Am79C30 are left disconnected on the Am79C32. This allows the user to convert from a data-only terminal to a voice/data terminal by simply replacing the Am79C30 with the Am79C32.

A serial port gives the user access to the B-channels of the Am79C32 multiplexer. This serial port may be used by data terminals and, with additional circuitry, provides access to the CCITT 'R' reference point.

The Am79C32 is controlled via a parallel interrupt-driven microprocessor bus interface by an external microprocessor. Using this interface, the microprocessor processes the D-channel information and programs the Am79C32 accordingly. This includes programming a multiplexer within the Am79C32 to route the B-channels as specified by the D-channel control information. The microprocessor can interrogate and program the Am79C32 via its mode, status, and error registers.

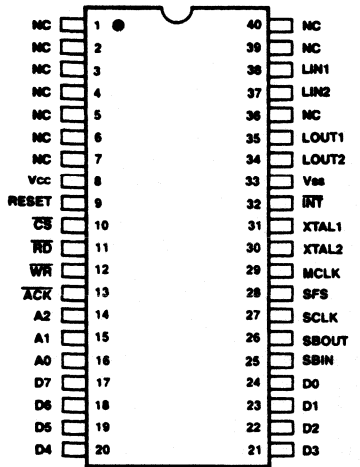


BD005850

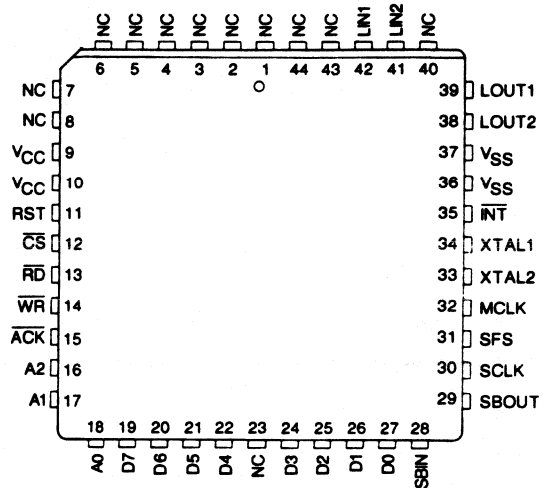
**Am79C32 IDC Block Diagram**

- MUX = Multiplexer
- LIU = Line Interface Unit
- OSC = Oscillator and Timing Circuitry
- DLC = Data Link Controller
- MPI = Microprocessor Interface
- MAP = Main Audio Processor

## CONNECTION DIAGRAMS



CD008050



CD008040

Note: Pin 1 is marked for orientation.

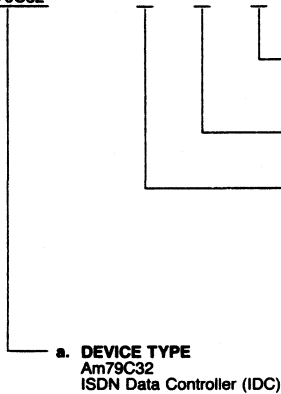
## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM79C32



- e. **OPTIONAL PROCESSING**  
Blank = Standard processing  
B = Burn-in
- d. **TEMPERATURE RANGE**  
C = Commercial (0 to +70°C)
- c. **PACKAGE TYPE**  
P = 40-Pin Plastic DIP (PD 040)  
D = 40-Pin Ceramic DIP (CD 040)  
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)
- b. **SPEED OPTION**  
Not Applicable
- a. **DEVICE TYPE**  
Am79C32  
ISDN Data Controller (IDC)

Valid Combinations	
AM79C32	PC, PCB, DC, DCB, JC, JCB

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am79C401

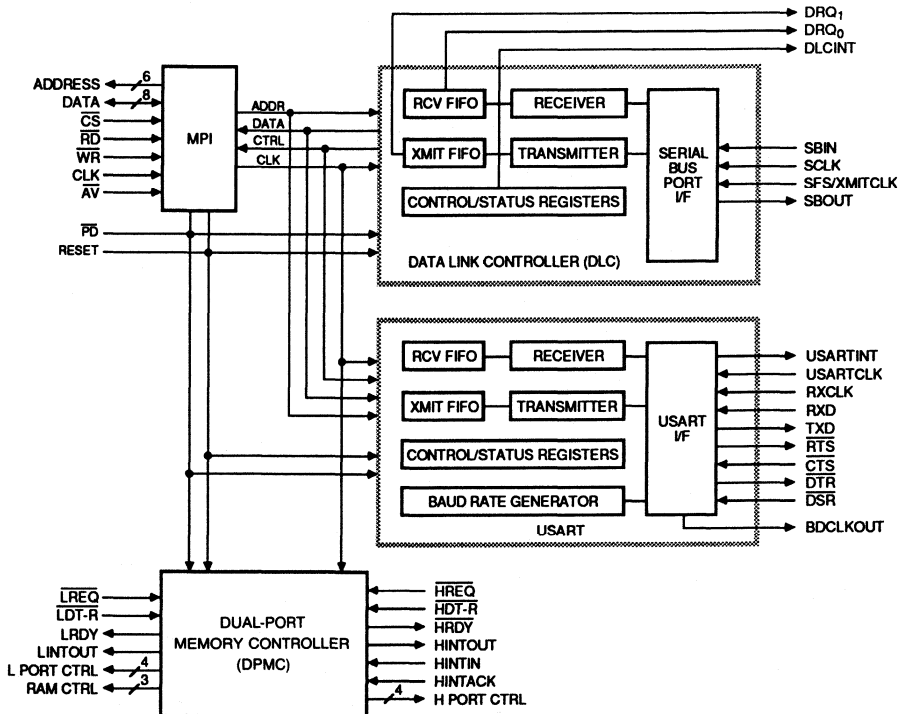
## Integrated Data Protocol Controller

### ADVANCE INFORMATION

#### DISTINCTIVE CHARACTERISTICS

- Data Link Controller
  - Bit-Oriented Protocols (HDLC, SDLC, LAPB, LAPD, and DMI)
  - Bit Insertion/Deletion
  - Residue Bits
  - Bit Inversion
  - 2.048 Mbit/sec Non-Multiplexed Mode
  - Multiplexed Mode supports connections to one of 31 time slots
  - 32-Byte Receive FIFO and 16-Byte Transmit FIFO
  - Programmable FIFO Thresholds
  - Full-Duplex with DMA or Interrupt requests
  - Programmable Minimum and Maximum Packet Size Checking
  - Abort Generation/Recognition
  - CRC Generation/Recognition
  - Flag or Mark Idle Generation/Recognition
  - Multiple (4 plus Broadcast) 8- or 16-Bit Address Recognition
  - Local Loopback and Remote Echo Modes
- USART
  - Superset of Industry-Standard 8250 UART
  - Four-Byte Receive/Transmit FIFOs
  - Data Rate: 300 to 56,000 bps
  - Internal Baud Rate Generator
  - Synchronous Option with External Clocks
  - Modem Control Lines (RTS, CTS, DSR, DTR)
  - 1, 1.5, or 2 Stop Bits
  - Break Recognition/Generation
  - Special Character Recognition
  - Parity Generator/Checker
  - Local Loopback Mode
  - Programmable, Maskable Interrupts
- Dual-Port Memory Controller
  - Dual-Port Memory Bus Request Arbitration
  - Programmable Inter-Processor Interrupts
- Am79C30 DSC and Am79C32 IDC Compatible
- CMOS Technology, Single +5 V Supply Voltage
- Power-Down Mode
- 68-Pin PLCC or LCC

#### BLOCK DIAGRAM



# Am79C31

Digital Exchange Controller (DEC)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Digital customer access for ISDN.
- Compatible with CCITT I-Series recommendations at 'S' and 'T' reference points.
- Applications for PABX Line Cards.
- ISDN CCITT 'S' reference interface:
  - Four-wire transceiver operation.
  - Supports point-to-point and point-to-multipoint configurations.
  - 192 kbps bit rate—64 kbps: voice/data B1-channel.
    - 64 kbps: voice/data B2-channel
    - 16 kbps: control/data D-channel.
    - 48 kbps: framing and maintenance
- IDI for control of the Am79C33
- Dual PCM highway:
  - Carries both B- and D-channels as programmable options.
  - Compatible with the SLAC PCM port.
  - Individual B- and D-channel time slot assignments.
- D-channel controller:
  - Level 1 physical layer.
  - Level 2 handling—Zero insertion/deletion.
    - Flag generation/detection.
    - CRC generation/checking.
  - 32 byte transmit and 32 byte receive FIFOs
- Parallel microprocessor interrupt-driven interface
- Test/maintenance loopbacks
- CMOS technology with single +5 V supply, TTL compatible

---

## GENERAL DESCRIPTION

The Am79C31 Digital Exchange Controller (DEC) provides the exchange termination functions for one ISDN subscriber line. The Am79C31 is compatible with the CCITT I-Series recommendations at the 'S' reference point. The user of this device may design PABX line cards which conform to the CCITT ISDN standards. The 'S' reference point interface provided on the Am79C31 is fully programmable via a microprocessor interface. A dual PCM interface is provided on the Am79C31 to gain direct access to the PABX line card backplane.

The Am79C31 'S' reference point interface supports the 192 kbps four-wire path to the subscriber TEs operating in either the point-to-point or point-to-multipoint configurations. The Am79C31 separates and combines the 192 kbps data stream into separate D- and B-channels, and inserts or extracts these channels on or off the PCM highway in the programmed time slot.

The D-channel can be processed (level 1 and partial level 2) in the Am79C31 at 16 kbps or 64 kbps and then passed to the external microprocessor for higher level processing. The D-channel can also be passed over the dual PCM highway with the B-channel data for centralized handling (the DLC processor in the Am79C31 is bypassed using this option). The microprocessor can program the Am79C31 to route the D- and B-channels as

desired and maintains supervision by interrogating status and interrupt registers contained within the Am79C31.

The Am79C31 dual PCM interface has independent control for the transmit and receive paths. The frame sync signal identifies the beginning of the frame and all time slots are referenced to it. The PCM interface will operate up to 8.192 Mbps, thus allowing up to 128 possible time slots at 64 kbps without blocking. During each frame two 64 kbps B-channels (8-bit time slots) and one 16 kbps or 64 kbps D-channel (2- or 8-bit time slots) may be transferred to/from the PCM highway. Time slot assignment and PCM highway selection are under control of the microprocessor.

To aid in maintenance of the system, several facilities are provided. Loopback is available at the 'S' and PCM interfaces. The B-channels may be monitored via the microprocessor interface.

Multiple Am79C31s under the control of one microprocessor can be contained on a single PABX line card. Thus multiple ISDN 'S' interface lines can be terminated on the one PABX line card with a microprocessor controlling the time slot assignments, activation and maintenance functions.

## GENERAL DESCRIPTION

The IDPC integrates several major components of an ISDN terminal or workstation in one flexible, cost-effective device.

The IDPC also provides a reduced-cost, high-performance solution for many existing non-ISDN telecommunications applications such as IBM Systems Network Architecture (SNA), AT&T Digital Multiplexed Interface (DMI), and X.25 terminals and workstations.

As shown in the Block Diagram, the IDPC is composed of several major functions: the Data Link Controller (DLC), the Universal Synchronous/Asynchronous Receiver/Transmitter (USART), Microprocessor Interface (MPI), and the Dual-Port Memory Controller (DPMC).

### Data Link Controller (DLC)

The DLC is a high-speed synchronous serial port supporting bit-oriented protocols such as HDLC, SDLC, LAPB, LAPD and DMI. The DLC supports CRC-CCITT recognition and generation, bit insertion and deletion, address recognition, abort recognition and detection, bit residue, and flag recognition and generation.

The DLC serial bus port can work in either a multiplexed or a non-multiplexed mode. In the non-multiplexed mode, the DLC performs like a standard serial communications controller supporting full-duplex transfers up to 2.048 Mbits/sec.

In the multiplexed mode, the DLC works with the serial bus port on the Am79C30 Digital Subscriber Controller (DSC) or Am79C32 ISDN Data Controller (IDC). The DLC provides access to any of the 64 Kbit/sec time slots in the Am79C30/Am79C32's 192 Kbit/sec serial bus. The DSC or IDC can then assign the time slots to any of the 64 Kbit/sec

channels on the 2B + D 'S' interface. The DLC can support logical connection to any of 31 time slots on the serial bus port.

The DLC supports data transfers via DMA, interrupts, or polled I/O. The DLC transmitter contains a 16-byte FIFO and the receiver contains a 32-byte FIFO to minimize interrupt latency and frequency of interrupts. The DLC provides both local loopback and a remote echo to support system testing.

### Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

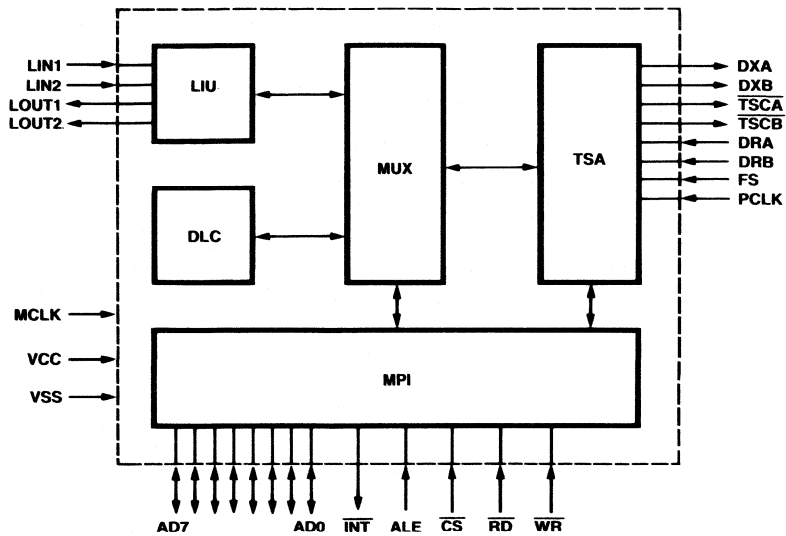
The USART contains a superset of 8250 UART features and supports both synchronous and asynchronous serial communications. The USART can operate full-duplex at speeds up to 56 Kbit/sec using the internal programmable baud rate generator or via external clock sources.

The USART supports break recognition and generation, parity generation/checking, and special character recognition. The USART supports 1, 1.5, or 2 stop bits. Modem control/handshake lines are provided for RTS, CTS, DSR, and DTR. For testing purposes, the USART contains a local loopback mode and "stick" parity.

### Dual-Port Memory Controller (DPMC)

The DPMC provides an on-board bus arbitration/controller to support the use of shared memory in multiprocessing applications such as intelligent communications controllers. The DPMC allows the implementation of shared memory using inexpensive static RAM. Interprocessor interrupts can be generated under software control.

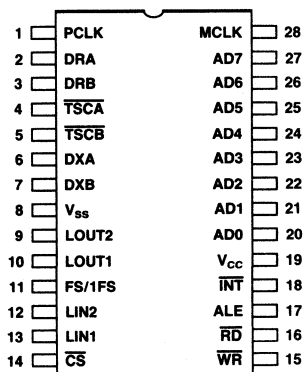




**Am79C31 DEC Block Diagram**

- LIU = Line Interface Unit
- DLC = Data Link Controller
- MUX = Multiplexer
- TSA = Time Slot Assigner
- MPI = Microprocessor Interface

## CONNECTION DIAGRAM

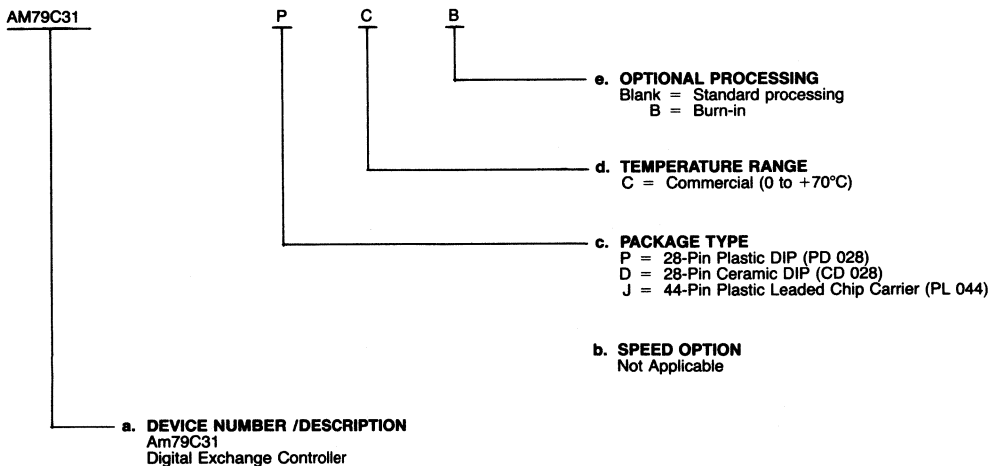


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



### Valid Combinations

AM79C31	PC, PCB, DC, DCB, JC, JCB
---------	---------------------------------

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am79C312

Digital Transceiver Controller (DTC)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Digital customer access for ISDN
- Compatible with CCITT I-Series recommendations at 'S' and 'T' reference points
- Applications for PABX Line Cards
- ISDN CCITT 'S' reference interface:
  - Four-wire transceiver operation
  - 192 kbps bit rate—64 kbps: voice/data B1-channel
    - 64 kbps: voice/data B2-channel
    - 16 kbps: control/data D-channel
    - 48 kbps: frame and maintenance
  - Point-to-point or point-to-multipoint operation
  - Fixed or adaptive thresholding with fixed or adaptive timing
- Dual PCM highway:
  - Carries both B- and D-channels as programmable options
  - Compatible with the Am790X-series Subscriber Line Audio-Processor Circuit's dual PCM port
  - Time Slot Assigner
    - Up to 128 time slots
    - Individual B- and D-channel time slot assignments
- Parallel microprocessor interrupt-driven interface
- Test/maintenance loopbacks
- CMOS technology with single +5 V Supply, TTL compatible

## GENERAL DESCRIPTION

The Am79C312 Digital Transceiver Controller (DTC) provides the exchange termination functions for one ISDN subscriber line. The Am79C312 is compatible with the CCITT I-Series recommendations at the 'S' reference point. The user of this device may design PABX line cards which conform to the CCITT ISDN standards. The 'S' reference point interface provided on the Am79C312 is fully programmable via a microprocessor interface. A dual PCM interface is provided on the Am79C312 to gain direct access to the PABX line card backplane.

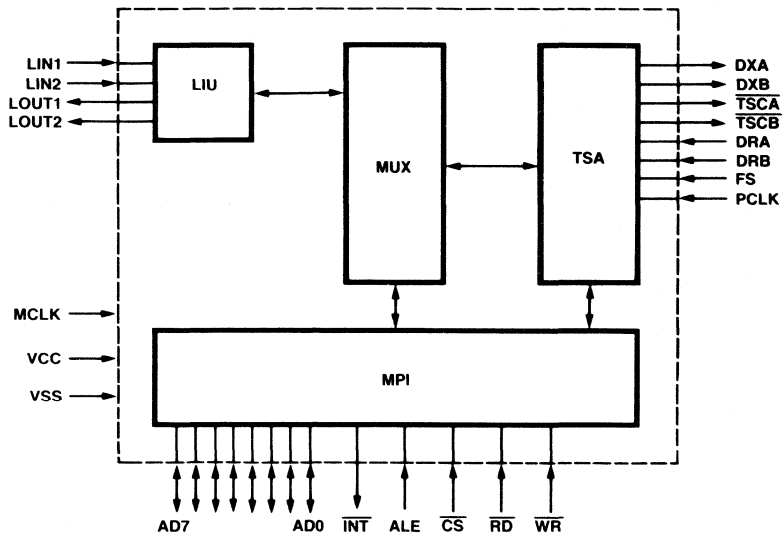
The Am79C312 'S' reference point interface supports the 192 kbps four-wire path to the subscriber TEs operating in either the point-to-point or point-to-multipoint configurations. The Am79C312 separates the 192 kbps data stream into separate D- and B-channels and inserts these channels onto the PCM highway in programmed time slots. Conversely, it extracts the D- and B-channels off of the PCM highway and inserts them onto the 192 kbps data stream.

The D-channel can be passed to the external microprocessor for testing purposes, or over the dual PCM highway with the B-channel data for centralized handling. The microprocessor can program the Am79C312 to route the D- and B-channels as desired and maintains supervision by interrogating status and interrupt registers contained within the Am79C312.

The Am79C312 dual PCM interface has independent control for the transmit and receive paths. The frame synchronization input signal identifies the beginning of the PCM frame and all time slots are referenced to it. The PCM interface will operate up to 8.192 Mbps, thus allowing up to 128 possible time slots at 64 kbps without blocking. During each PCM frame, two 64 kbps B-channels (8-bit time slots) and one 16 kbps or 64 kbps D-channel (2- or 8-bit time slots) may be transferred to/from the PCM highway. Time slot assignment and PCM highway selection are under control of the microprocessor. Data transfers between the PCM highway and 'S' interface are internally synchronized.

To aid in maintenance of the system, several facilities are provided. Loopback is available at the 'S' and PCM interfaces. The B-channels may be monitored via the microprocessor interface.

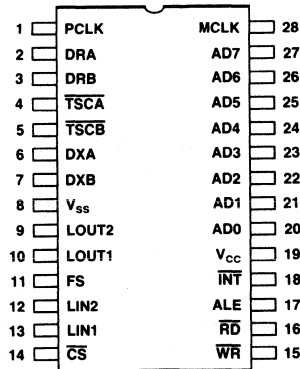
Multiple Am79C312s under the control of one microprocessor can be contained on a single PABX line card. Thus multiple 'S' interface lines can be terminated on the one PABX line card with a microprocessor controlling the time slot assignments, activation and maintenance functions.



**Am79C312 DTC Block Diagram**

- LIU = Line Interface Unit
- MUX = Multiplexer
- TSA = Time Slot Assigner
- MPI = Microprocessor Interface

## CONNECTION DIAGRAM



## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM79C312

P

C

B

- e. **OPTIONAL PROCESSING**  
 Blank = Standard processing  
 B = Burn-in

- d. **TEMPERATURE RANGE**  
 C = Commercial (0 to +70°C)

- c. **PACKAGE TYPE**  
 P = 28-Pin Plastic DIP (PD 028)  
 D = 28-Pin Ceramic DIP (CD 028)  
 J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

- b. **SPEED OPTION**  
 Not Applicable

- a. **DEVICE NUMBER/DESCRIPTION**  
 Am79C312  
 Digital Transceiver Controller

### Valid Combinations

Valid Combinations	
AM79C312	PC, PCB, DC, DCB, JC, JCB

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am7936

Subscriber Power Controller (SPC)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- CCITT ISDN-compatible switched mode power controller
- 70 V bipolar technology
- Accommodates both galvanically isolated and non-isolated configurations
- Wide input voltage range (15 – 65 V)
- Fixed (5 V DC) or programmable output voltage
- Polarity reversal with external components
- Low-power detection
- Automatic-load disconnect at programmed LOW input voltage level
- Clock-synchronization input
- Fixed and programmable under-voltage protection
- Microprocessor reset output
- Programmable reset voltage level
- Low power dissipation

## GENERAL DESCRIPTION

The Am7936 Subscriber Power Controller (SPC) is primarily designed to provide a stable, regulated 5 V DC supply to the ICs contained in the Terminal Equipment (TE1). It is fully compatible to the CCITT power recommendations for the 'S' interface. The Am7936 can also be used in Network Terminating (NT) equipment to supply the NT ICs with a regulated DC voltage and/or the 'S' interface with power. The input voltage supply to the Am7936 can be provided by a local line or, in the absence of local power, a battery or via the exchange from one or two pairs of subscriber lines; for example, the 'S', 'T', or 'U' reference points. The Am7936, coupled with a few external components, converts the unregulated DC input to a regulated DC output.

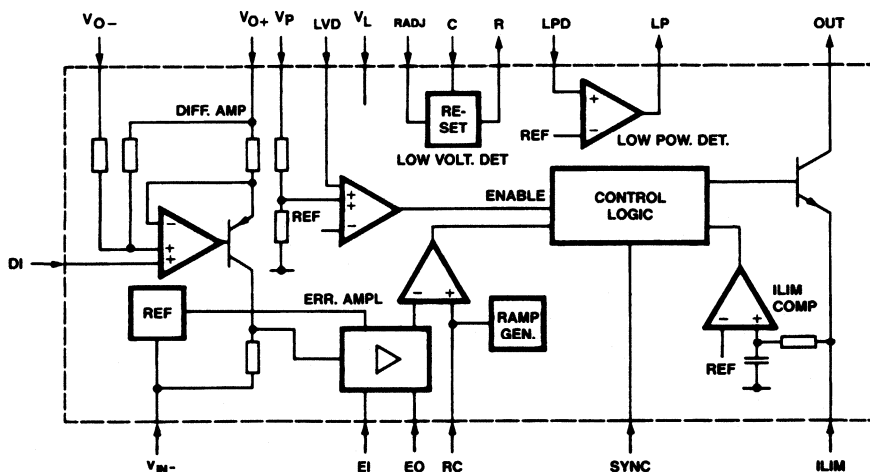
The Am7936 can be operated in both the non-isolated and the galvanically isolated configurations. In the non-isolated configuration, the input voltage is physically connected to the output voltage via the Am7936 and an external inductor.

This configuration may be used for TE voice-only applications such as feature phones, with no local power supplied.

For TEs which have a local ground, a galvanically isolated power supply is required to avoid interference caused by noisy grounds or longitudinal currents induced from power lines. An external transformer is used to electrically isolate the input and output voltages of the Am7936. Galvanic isolation applies when a locally powered data terminal is attached via the Am79C30's serial port to communicate over the 'S' interface.

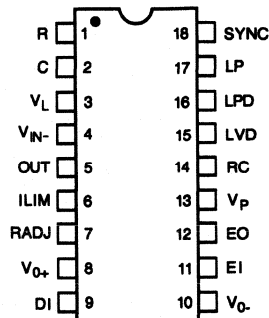
The Am7936 has been developed specifically for CCITT-compatible configurations; however, its versatile design makes it useful in numerous other applications.

## BLOCK DIAGRAM



BD006432

## CONNECTION DIAGRAM



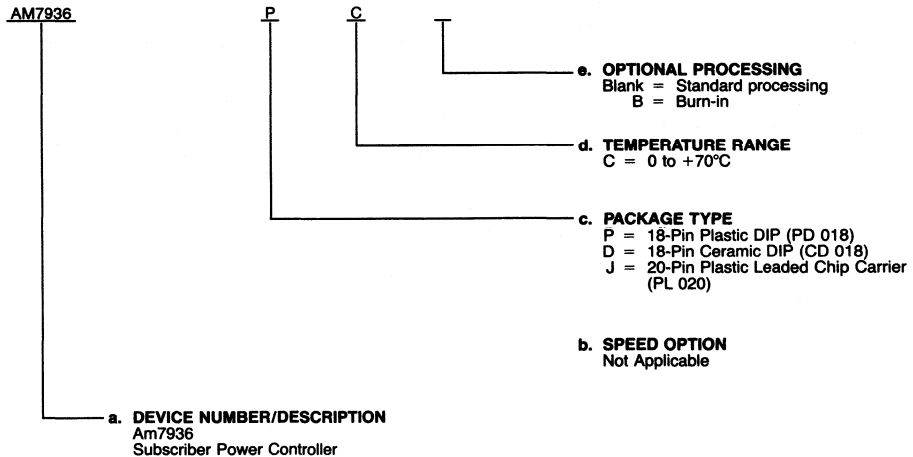
CD009581

Note: Pin 1 is marked for orientation.

## ORDERING INFORMATION Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM7936	PC, PCB, DC, DCB, JC, JCB

# Am7938

Quad Exchange Power Controller (QEPC)

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Supplies power for up to four digital telephone lines
  - Conforms to the CCITT recommendations for power feed at the 'S' reference point
  - Applications for Intelligent NTs and PABX/Central Office line cards
  - Supports point-to-point and point-to-multipoint configurations
  - Built-in battery control circuit for -40 V operation
  - Each of the four lines is individually controlled
  - Status detectors for each line driver (open loop current overload, reverse current, low voltage, and thermal overload)
  - Programmable current limiting
  - Automatic shutdown of shorted lines when  $T_j > 140^\circ\text{C}$
  - Thermal shutdown for  $T_j > 150^\circ\text{C}$
  - Microprocessor-compatible interface
  - High-voltage bipolar technology allows battery voltages up to 65 V
  - Output current up to 150 mA per driver
- 

## GENERAL DESCRIPTION

The Am7938 Quad Exchange Power Controller (QEPC) provides a regulated 40 V power source for up to four line interfaces. The power source to the Am7938 is a local battery or a centralized regulated power supply. The Am7938 can reside in intelligent NTs or PABX/Central Office line cards. It can operate in point-to-point and point-to-multipoint configurations. Via the Am7938's microprocessor interface, each line powered is individually controlled and monitored. The power to each line can be switched off independently. Hence, overloads and faults are easy to detect and localize even in a large system.

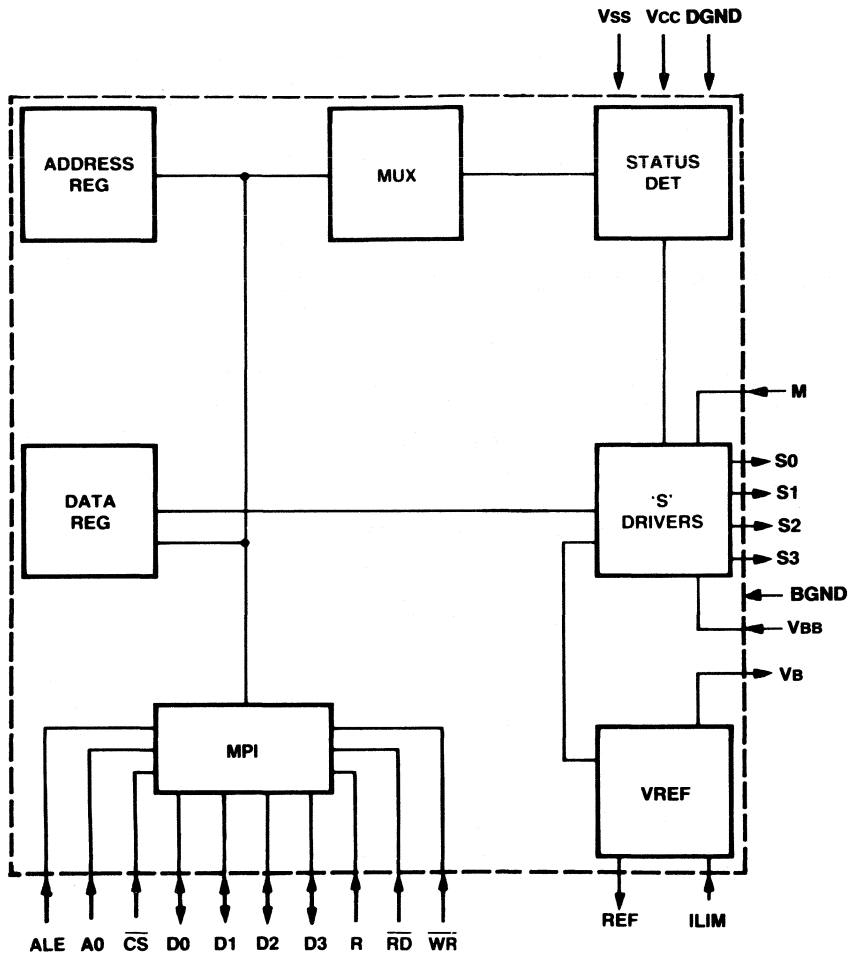
The Am7938 provides the microprocessor the following status conditions on each line:

Low output voltage, open-loop, current overload, reverse-current, thermal overload, and normal load.

Current limit and thermal shut-down protection circuits make the Am7938 virtually overload proof; however, in certain applications, additional external protection circuits may be required.

The Am7938 has been developed specifically for CCITT-compatible ISDN configurations; however, its versatile design makes it useful in numerous other application areas.

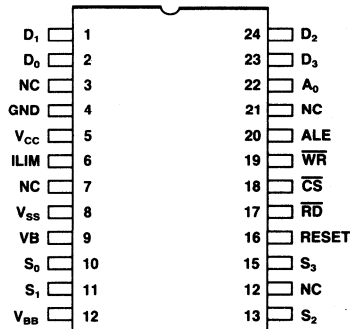




Am7938 QEPC Block Diagram

Address Reg = Address Register  
 MUX = Multiplexer  
 Status Det = Status Detection  
 Data Reg = Data Register  
 MPI = Microprocessor Interface  
 VREF = Voltage Reference

## CONNECTION DIAGRAM

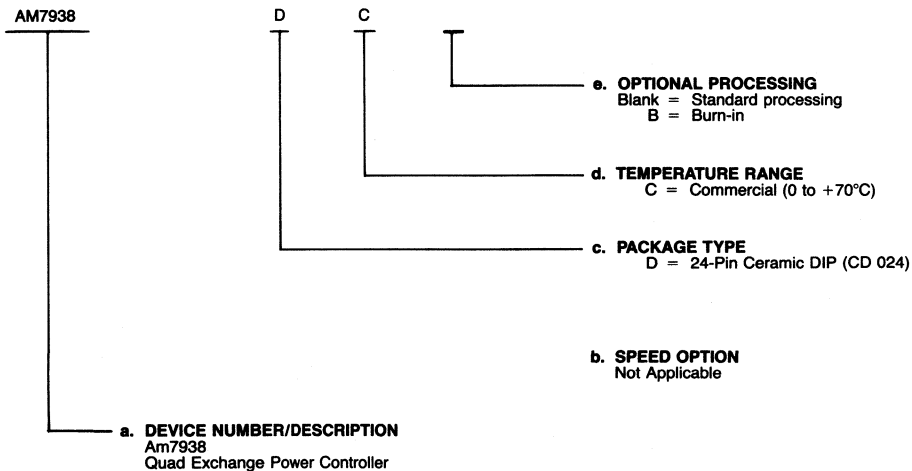


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7938	DC

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# **VOICE SWITCHING PRODUCTS**

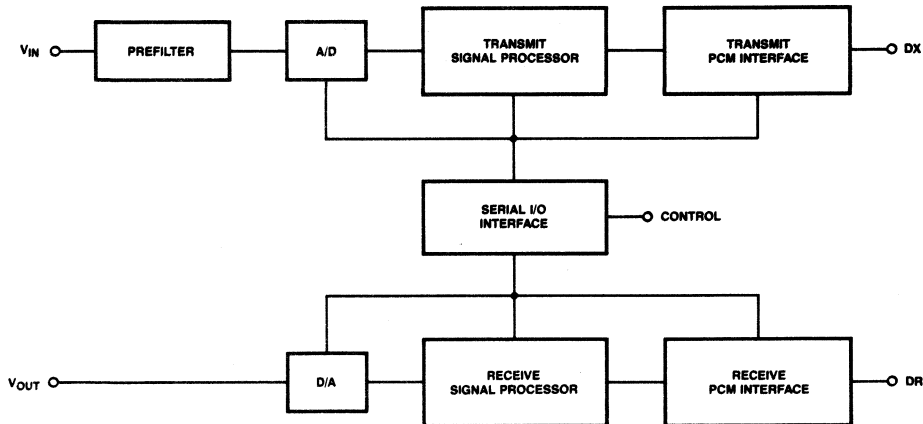
# THE FIRST TELECOMMUNICATION CODEC/FILTER UTILIZING STATE-OF-THE-ART MICROPROCESSOR TECHNOLOGY TO SOLVE YOUR LINE-CARD PROBLEMS

Advanced Micro Devices' Am7901A/B and Am7905A Subscriber Line Audio-Processing Circuits (SLAC), designed using digital signal processing techniques, employ digital filters to provide many system advantages. Through application of advanced LSI technology, AMD has incorporated the codec/filter and other line-card functions into the SLAC.

AMD's SLAC permits the digital switch designer to off-load some processing from other system processors to the line-card, and thus improve system efficiency while reducing cost.

No other approach to line-card design allows as much flexibility and reliability.

**SLAC Block Diagram**



MMC-197

# Am7901A/B

Subscriber Line Audio-Processing Circuit  
WORLD-CHIP™  
PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Combination Codec and filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic time slot assignment
- Only two external components (non-precision)
- Dual PCM ports
- 4.096 MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable linear,  $\mu$ -law (Am7901A) or  $\mu$ -law, A-law (Am7901B)

## GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

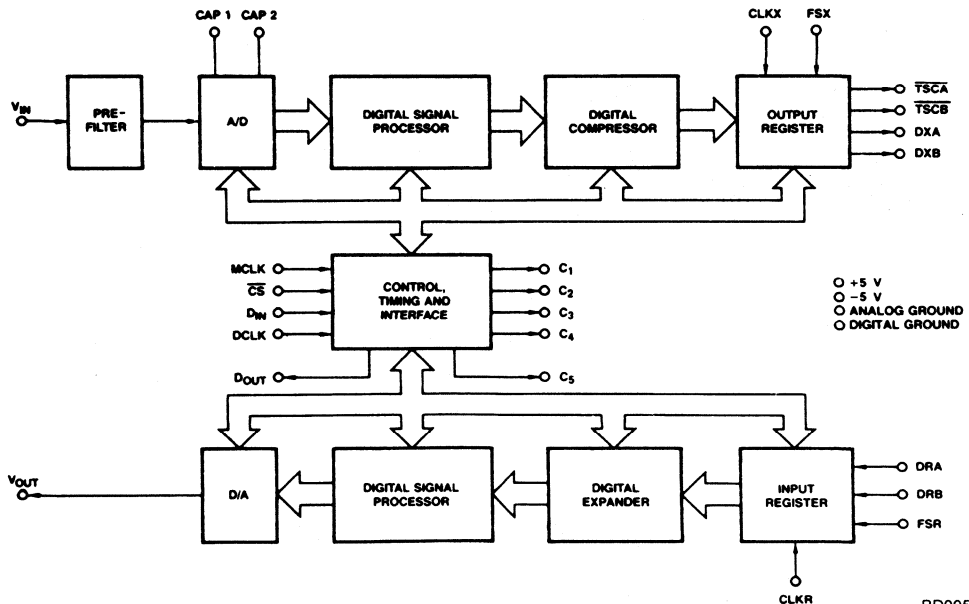
The transmit section contains an anti-aliasing filter, an interpolative A/D converter, and a digital signal processor. The analog signals received are converted and digitally processed to generate either 16-bit linear or 8-bit  $\mu$ -law codes (Am7901A), or 8-bit  $\mu$ -law or A-law codes (Am7901B).

Either one of two output ports may be selected for PCM data transmission.

The receive section contains a digital signal processor and a D/A converter. Either 16-bit linear or 8-bit  $\mu$ -law codes (Am7901A), or 8-bit  $\mu$ -law or A-law codes (Am7901B) are received, processed, and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

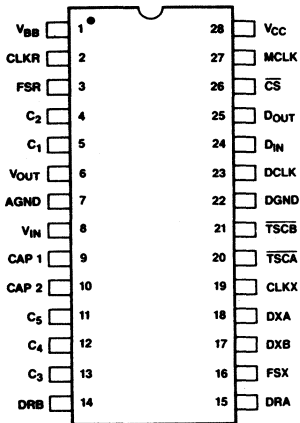
The control I/O provides a microprocessor-compatible serial interface, and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of 32 commands.

## BLOCK DIAGRAM

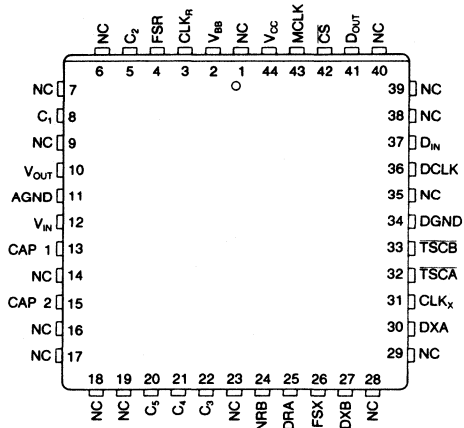


BD005161

## CONNECTION DIAGRAMS



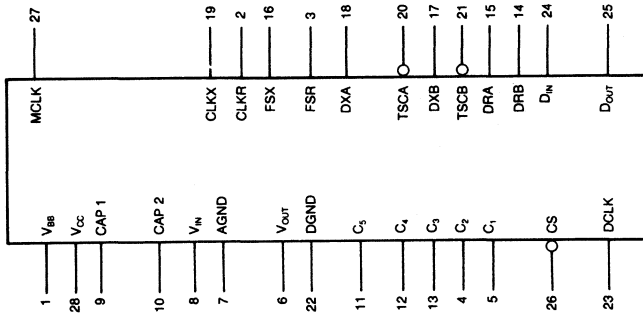
CD005871



CD007041

## LOGIC SYMBOL

### DIPs



LS001891

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM7901A

P

C

- e. **OPTIONAL PROCESSING**  
Blank = Standard processing

- d. **TEMPERATURE RANGE**  
C = Commercial (0 to +70°C)

- c. **PACKAGE TYPE**  
P = 28-Pin Plastic DIP (PD 028)  
D = 28-Pin Ceramic DIP (CD 028)  
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

- a. **DEVICE NUMBER/DESCRIPTION**

Am7901A (Linear,  $\mu$ -Law)  
Am7901B (A-Law,  $\mu$ -Law)  
Subscriber Line Audio-Processing Circuit (SLAC) WORLD-CHIP

### Valid Combinations

Am7901A	PC, DC, JC
Am7901B	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am7905A

Subscriber Line Audio-Processing Circuit  
WORLD-CHIP™  
PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Combination Codec and filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic time slot assignment
- Only two external components (non-precision)
- Dual PCM ports
- 4.096 MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable  $\mu$ -law or A-law
- 24-pin DIPs

## GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

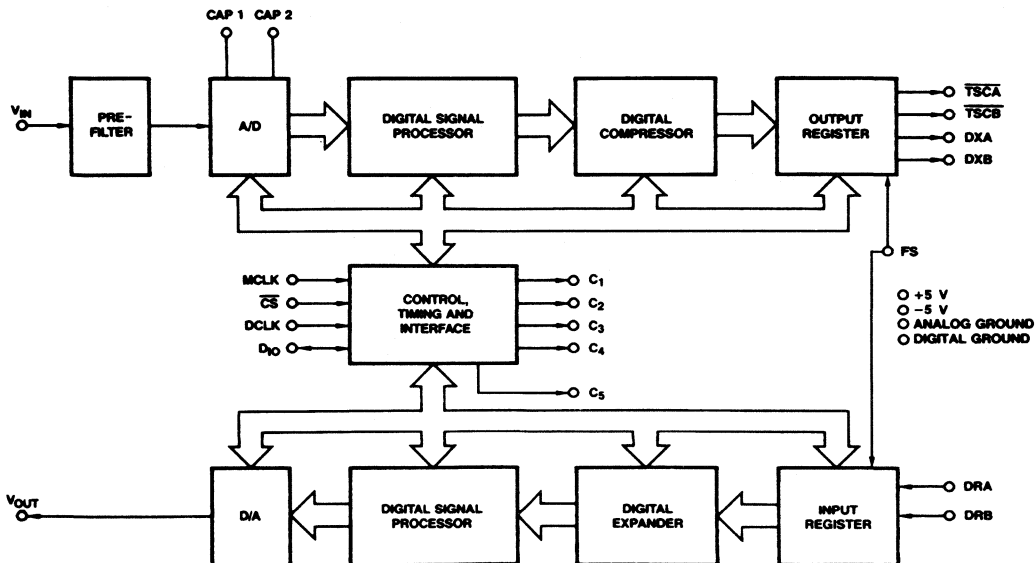
The transmit section contains an anti-aliasing filter, an interpolative A/D converter, and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit  $\mu$ -law or A-law codes. Either

one of two output ports may be selected for PCM data transmission.

The receive section contains a digital signal processor and a D/A converter. Either 8-bit  $\mu$ -law or A-law codes are received, processed, and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

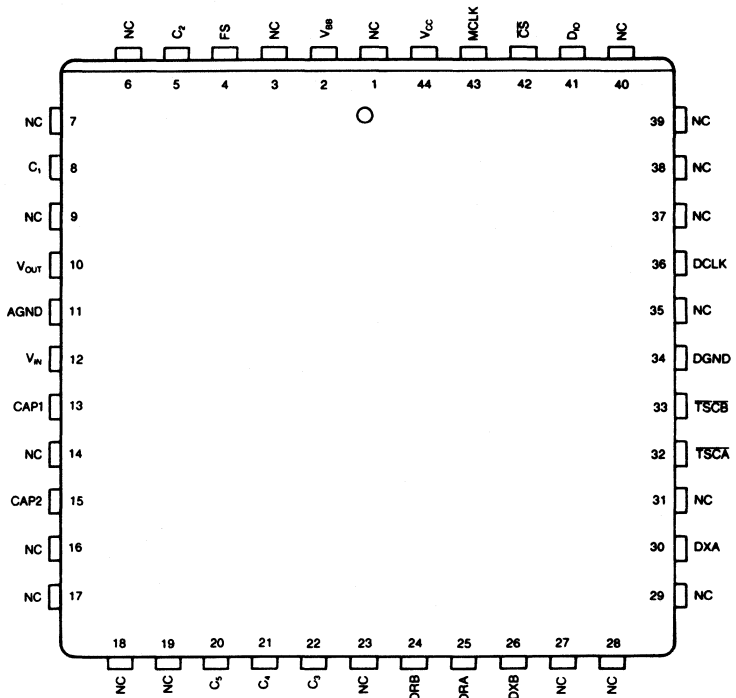
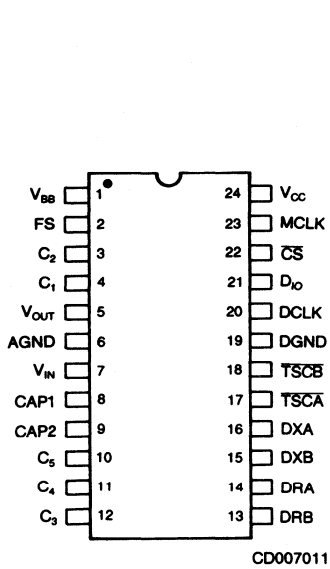
The control I/O provides a microprocessor-compatible serial interface, and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of 34 commands.

## BLOCK DIAGRAM

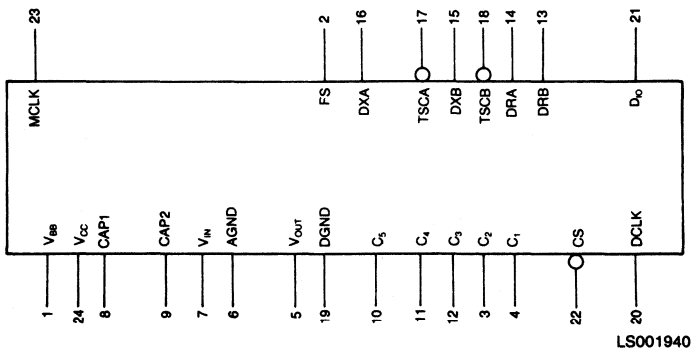


BD005381

## CONNECTION DIAGRAMS Top View



## LOGIC SYMBOL DIPs



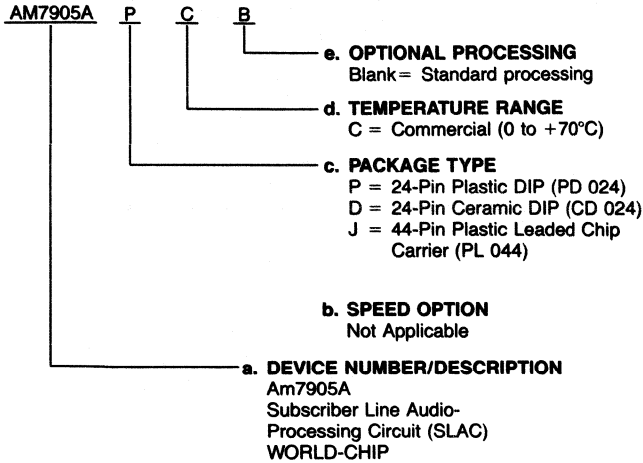


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7905A	PC, DC, JC

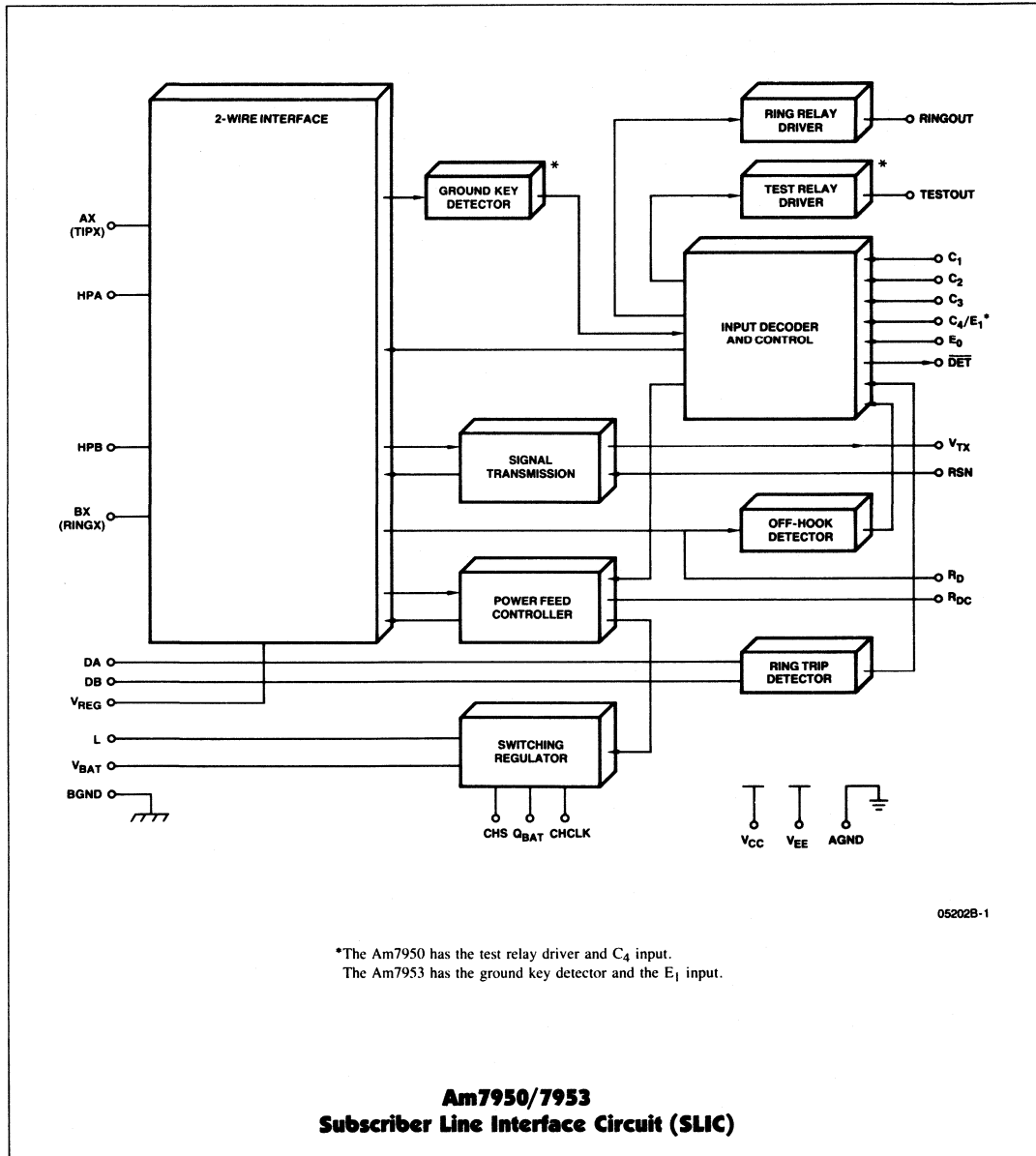
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# THE FIRST COMPLETE MONOLITHIC SLIC PERFORMS ALL BORSHT FUNCTIONS!

Designed using high-voltage bipolar technology with precision thin-film resistors, Advanced Micro Devices' Am7950/7953 Subscriber Line Interface Circuits (SLIC) contain an innovative set of features, providing many benefits for system designers.

Along with improved system performance and special signaling functions, AMD's Am7950/7953 SLIC offers dramatic cost and power savings.



\*The Am7950 has the test relay driver and C<sub>4</sub> input.  
The Am7953 has the ground key detector and the E<sub>1</sub> input.

## Am7950/7953 Subscriber Line Interface Circuit (SLIC)

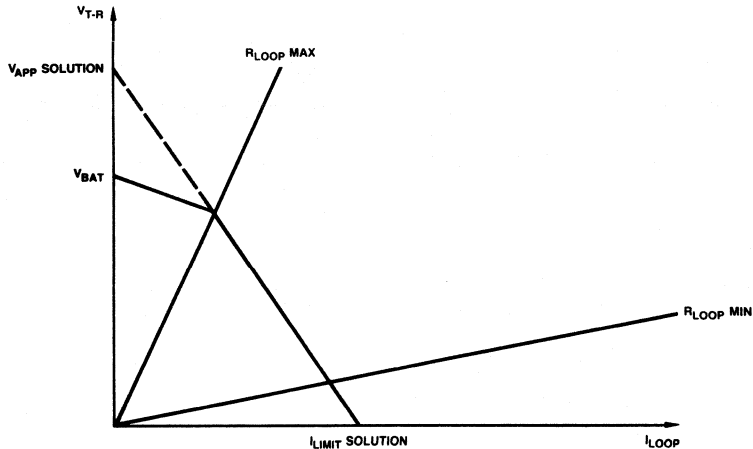
## NEW BATTERY FEED SYSTEM SOLVES POWER DISSIPATION PROBLEMS!

A patented new battery feed system allows users of AMD's Am7950 SLIC previously unattainable degrees of design flexibility and performance.

The Am7950 uses the DC loop current as a control variable in a feedback loop to establish a modified DC feed voltage *without excess power dissipation*. Now you can design resistive feed systems where the feed resistance is

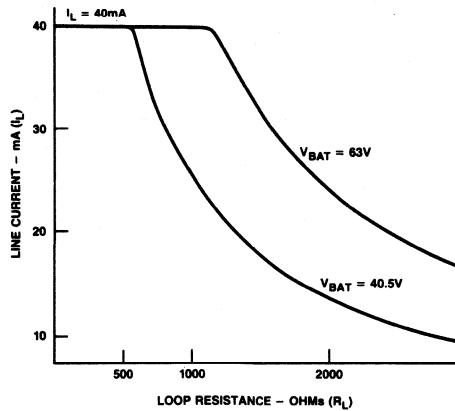
programmable and independent of the actual battery. This minimizes system power dissipation and keeps the loop current independent of the battery variations.

The Am7953 allows the DC feed current to be programmed with external resistors. The feed current is independent of battery variations and loop length.



05202B-2

**Am7950 Line Feed Characteristics**



**Am7953 SLIC Line Feed Characteristics**

05202B-3

# Am7950

## Subscriber Line Interface Circuit

PRELIMINARY

### DISTINCTIVE CHARACTERISTICS

- Programmable line-feed impedance
- Programmable loop detect threshold
- Line feed characteristics independent of battery variations
- On-chip switching regulator for low power dissipation
- Low standby power
- Two-wire impedance set by single external impedance

### GENERAL DESCRIPTION

The Am7950 Subscriber Line Interface Circuit (SLIC) performs the telephone line interface functions required in both Central Office and PABX environments. The full range of signal transmission, battery feed, and loop supervision functions are performed. Signal transmission performance is compatible with North American and CCITT recommendations. Overvoltage protection and ringing are provided by means of external networks.

The signal transmission functions include both 2-to-4-wire and 4-to-2-wire conversion. The 2-wire termination impedance is programmable with a single external impedance, which may be complex. The companion AMD SLAC (Subscriber Line Audio Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the SLAC is not used, most codec/filter sets provide an uncommitted op amp which may be used for this purpose.

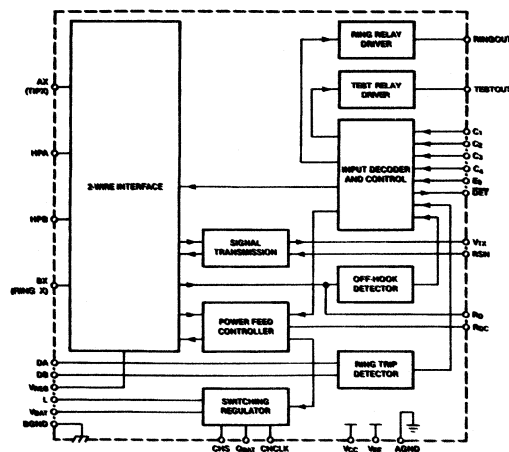
The battery-feed architecture makes the DC-feed resistance programmable with external resistors. Furthermore, the open-circuit feed voltage and the feed resistance are independent of battery variations. Loop currents up to 70 mA are recommended, although higher loop currents are possible.

A Polarity Reversal function is provided which transposes the normal voltage sense of the A(TIP) and B(RING) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode limits loop current and cuts power dissipation while allowing the full complement of supervisory functions to be utilized. The output amplifiers are powered by an internal switching regulator in order to also reduce power consumption.

The supervisory functions of off-hook detection and ring trip detection are read through a single, TTL-compatible output. To eliminate noise induced errors, the off-hook detector signal may be filtered, and has a threshold adjusted by means of external components. Additional supervisory functions put the A(TIP) lead into an open-circuit or high-impedance state suitable for application in ground-start systems. Similarly, both the A(TIP) and B(RING) leads may be open circuited to clear relays, recover from line faults, or turn off out-of-service lines. Two relay drivers are provided for the test and Ring relay functions.

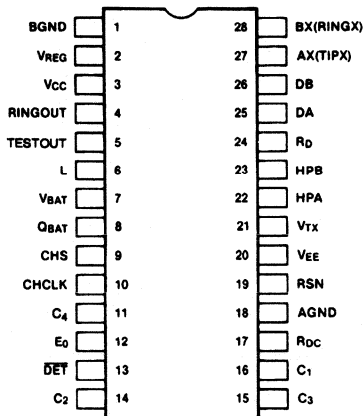
The SLIC's user-programmable states are controlled by a 4-bit TTL-compatible digital code. These control inputs are designed to easily interface to popular single-chip microcomputers such as the AMD Am8051.

### BLOCK DIAGRAM



BD005491

## CONNECTION DIAGRAM



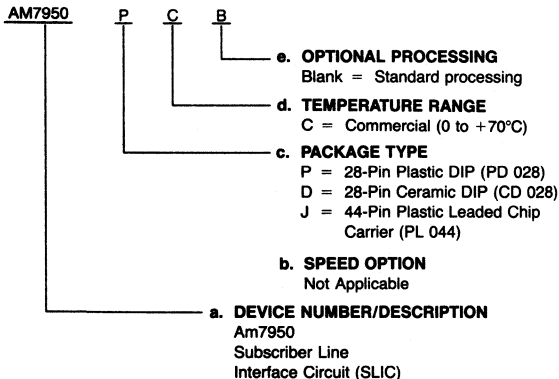
CD007071

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7950	DC

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am7953/Am7957

## Subscriber Line Interface Circuit

### ADVANCE INFORMATION

#### DISTINCTIVE CHARACTERISTICS

- Programmable constant current (Am7953), or constant Voltage Linear Feed (Am7957)
- Programmable loop detect threshold
- Ground key detect
- Line feed characteristics independent of battery variations
- On-chip switching regulator for low power dissipation
- Low standby power
- Two-wire impedance set by single external impedance

#### GENERAL DESCRIPTION

The Am7953/57 Subscriber Line Interface Circuit (SLIC) performs the telephone line interface functions required in both Central Office and PABX environments. The full range of signal transmission, battery feed, and loop supervision functions are performed. Signal-transmission performance is compatible with North American and CCITT recommendations. Overvoltage protection and ringing are provided by means of external networks.

The signal transmission functions include both 2-to-4-wire and 4-to-2-wire conversion. The 2-wire termination impedance is programmable with a single external impedance, which may be complex. The companion AMD SLAC (Subscriber Line Audio Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the SLAC is not used, most codec/filter sets provide an uncommitted op amp which may be used for this purpose.

The Am7953's battery-feed architecture makes the DC-feed current programmable with external resistors. The feed current is independent of battery variations.

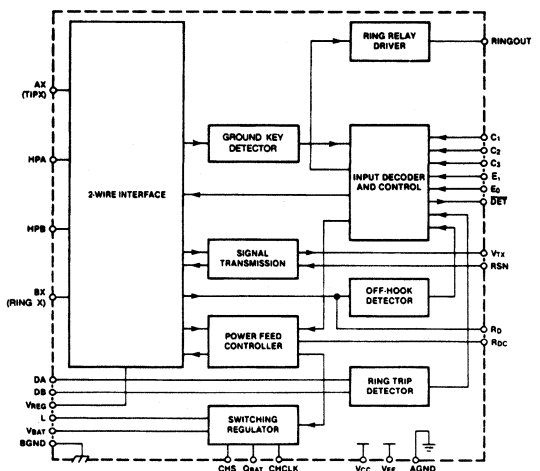
In the Am7957, the battery-feed architecture makes the DC feed resistance programmable with external resistors. Furthermore, the open circuit feed voltage and feed resistance are independent of battery variations. Loop currents up to 70 mA are recommended, although higher loop currents are possible.

A Polarity Reversal function is provided which transposes the normal voltage sense of the A(TIP) and B(RING) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode limits loop current and cuts power dissipation while allowing the full complement of supervisory functions to be utilized. The output amplifiers are powered by an internal switching regulator in order to also reduce power consumption.

The supervisory functions allow for off-hook detection, ground key detection, and ring trip detection. The outputs of these detectors are read through a single, TTL-compatible output. To eliminate noise-induced errors, the off-hook detector signal may be filtered, and has a threshold adjusted by means of external components. Additional supervisory functions put the A(TIP) lead into an open-circuit or high-impedance state suitable for application in ground-start systems. Similarly, both the A(TIP) and B(RING) leads may be open circuited to clear relays, recover from line faults, or shut off out-of-service lines. A relay driver is provided for the Ring-relay function.

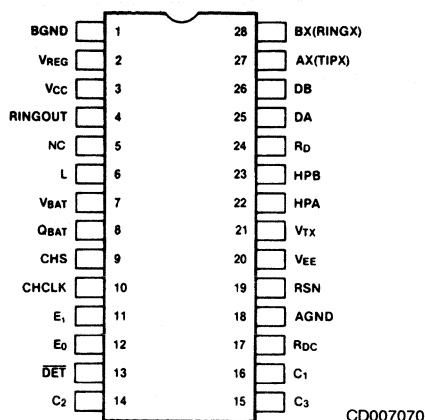
The Am7953/57 SLIC's user-programmable states are controlled by a 3-bit TTL-compatible digital code. The detector output is controlled by a selector bit and an enable bit. These lines are TTL-compatible.

#### BLOCK DIAGRAM



BD005490

## CONNECTION DIAGRAM



## PIN DESCRIPTION

**VCC**  
+5-volt power supply

**VEE**  
-5-volt power supply

**AGND Ground**  
Analog (quiet) and digital ground

**BGND Ground**  
Battery (power) ground

**VBAT**  
Battery supply

**AX(TIPX) (Output)**  
Output of A(TIP) power amplifier

**BX(RINGX) (Output)**  
Output of B(RING) power amplifier

**HPA**  
A(TIP) side of high-pass filter capacitor

**HPB**  
B(RING) side of high-pass filter capacitor

**RSN Receive Summing Node**  
The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks which program receive gain. 2-wire impedance and feed resistance all connect to this node.

**VTX Transmit Audio (Output)**  
This output is a unit-gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the 2-wire input-impedance-programming network connects here.

**E0 Read Enable**  
A logic HIGH enables  $\overline{DET}$ . A logic disables  $\overline{DET}$ .

**E1 Ground Key Enable (Input)**  
When  $E_0$  is HIGH,  $E_1 = \text{HIGH}$  connects the ground key detector to  $\overline{DET}$ , and  $E_1 = \text{LOW}$  connects the off-hook or ring trip detector to  $\overline{DET}$ .

**DET Detector (Output)**  
When enabled, a logic LOW indicates that the selected detector is tripped. The detector is selected by the logic inputs

( $C_1 - C_3, E_1$ ). The output is open-collector with a built-in pullup resistor.

**RD**  
Threshold modification and filter point for the off-hook detector. Also sets current in disable mode to 1.5 times the off-hook threshold.

**RDC**  
Connection point for DC feed resistance programming network. The other end of the network connects to the receiver summing node (RSN). The sign of  $V_{RDC}$  is minus for normal polarity and plus for reverse polarity. The magnitude is typically 2.5 volts except during voltage-limited output.

**CHS Chopper Stabilization (Input)**

**CHCLK Chopper Clock (Input)**  
Input to switching regulator (TTL compatible). Frequency = 256 kHz (nominal).

**L Switching Regulator Power Transistor (Output)**  
Connection point for 1.0-mH inductor and anode of catch diode. This pin will have up to 60 volts pulse waveform on it. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

**VREG Regulated Voltage (Input)**  
Provides negative power supply for power amplifiers. Connection point for inductor, filter capacitor and chopper stabilization.

**QBAT Filtered Battery Supply**  
For the signal processing circuits

**C1 - C3 Decoder (Inputs)**  
TTL compatible.  $C_3$  is MSB and  $C_1$  is LSB

**RINGOUT Ring Relay Driver (Output)**  
Sourcing from  $V_{CC}$

**DA Negative (Input)**  
Negative input to ring trip comparator

**DB Positive (Input)**  
Positive input to ring trip comparator





# **NETWORKING PRODUCTS**

# Networking System Overview

Advanced Micro Devices produces a set of LSI devices that provides the IEEE-802.3/Ethernet/CHEAPERNET system designer, and designers of IEEE-802.3/Ethernet compatible products, a low-cost physical and link level interface to the Ethernet Bus.

The Am7990 Ethernet interface family is being designed using a combination of MOS and IMOX™ bipolar technologies. This family consists of the Am7990 Local Area Network Controller for Ethernet (LANCE), the Am7992B Serial Interface Adapter for Ethernet (SIA) and the Am7996 Ethernet Transceiver. As shown in Figure 1, the Am7990 family provides the complete interface between the device System Bus and the Ethernet Cable.

The Am7990 LANCE is a 10M-bit/sec MOS device in a 48-pin package, optimized to perform the link level Ethernet protocol. The CSMA/CD network access, memory management (onboard DMA), error reporting, packet handling, and micro-processor interface functions also reside in the LANCE.

The Am7992B Serial Interface Adapter provides Manchester encoding and decoding of the serial bit stream and interfaces the TTL output of the LANCE to the differential inputs of the transceiver. It has an on-board phase locked loop to recover clock from an incoming signal, and can use an external crystal oscillator or TTL inputs to provide clock for transmission.

Coupling the Ethernet Node to the Ethernet Cable requires a transceiver. The Am7996 IEEE-802.3/Ethernet Transceiver provides Collision Detect, Jabber Control, and Line Driver/Receiver functions. The Am7995, along with appropriate isolation and an Off-the-Shelf DC to DC converter, can be used to implement a cost effective IEEE-802.3/Ethernet Rev 2 compatible transceiver.

## BASIC SYSTEM OPERATION

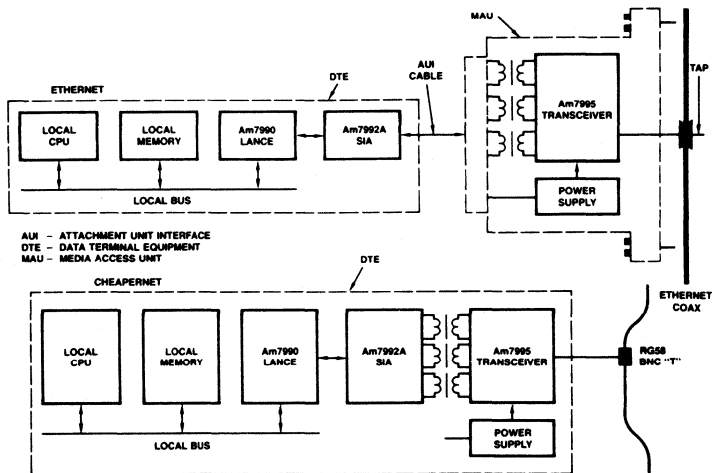
Ethernet is a send and receive half duplex system. The node must function in either transmit or receive mode at any instant in time. Before transmission the node must be sure there is no contention for the bus. The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two nodes attempt to transmit at the same time, the signals will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit and detect the collision. Both continue to transmit for a predetermined length of time to "jam" the network, ensuring all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary back-off" algorithm implemented in the LANCE before attempting to transmit again. This minimizes the possibility of collision on retransmission.

## TRANSMIT MODE

In the transmit mode, the LANCE initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with a preamble and sync pattern, then calculates and appends a 32-bit CRC.

This packet is transmitted serially to the SIA. The Manchester encoder in the SIA takes the transmitted data from the LANCE and creates the Manchester encoded differential signals TRANSMIT+ and TRANSMIT- to drive the Transceiver cable. These differential signals are coupled through the transceiver cable, transceiver, and on to the Ethernet coaxial cable.

Figure 1. Typical Ethernet/Cheapernet Node



AF000473

## RECEIVE MODE

When carrier is present on the Ethernet coax, the Transceiver will create the differential signals RECEIVE+ and RECEIVE-. These inputs to the SIA are decoded by the Manchester decoder. A phase locked loop synchronizes to the Ethernet Preamble, allowing the decoder to recover clock and data from the encoded signals. These two signals are supplied to the LANCE as the TTL signals RECEIVE DATA and RECEIVE CLOCK. In addition, the SIA creates the signal CARRIER PRESENT while it is receiving data from the cable, indicating to the LANCE that receive data and clock are available. When these signals reach the LANCE, the CRC is calculated and compared to the CRC checksum at the end of the packet. If the calculated CRC doesn't agree with the packet CRC, an error bit is set and an interrupt generated to the microprocessor.

## ADDRESSING

There are three addressing modes. The first is physical addressing which requires a comparison of the 48-bit destination address in the packet with the node address programmed into the LANCE during initialization. The second mode is multi-cast addressing. This mode can be useful when sending packets to all of one type of a device simultaneously on the network, or for a broadcast situation where all nodes on the network

receive the packet. In the final "promiscuous" mode of operation, a node will accept all packets on the coax regardless of their destination address.

## ERROR REPORTING

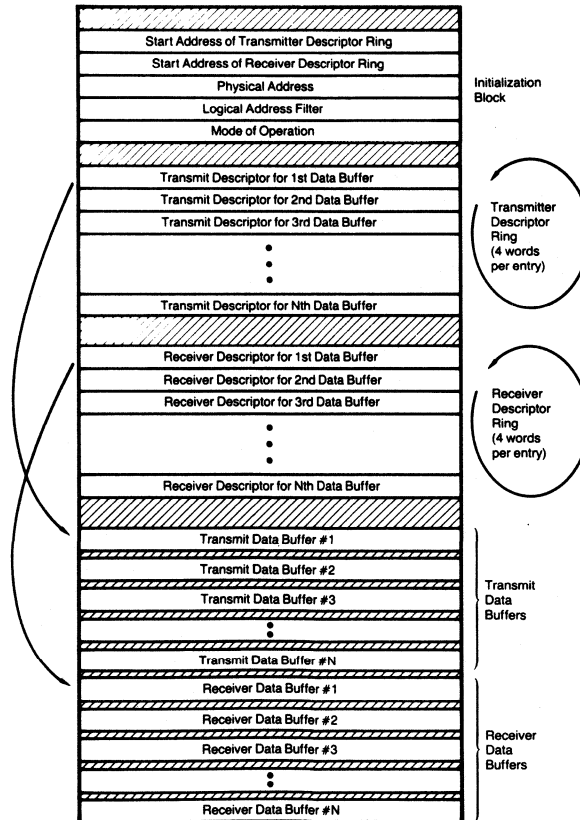
Extensive error reporting is provided by the LANCE through microprocessor interrupt and error bits in a status register. The following are the significant error conditions:

- CRC error on receive
- Babbling error
- Missed packet
- Memory error

## BUFFER MANAGEMENT

A key feature of the LANCE and its on-board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management consists of circular task queues, called descriptor rings, for transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring awaiting execution by the LANCE. (Figure 2)

Figure 2. LANCE/Processor Memory Interface



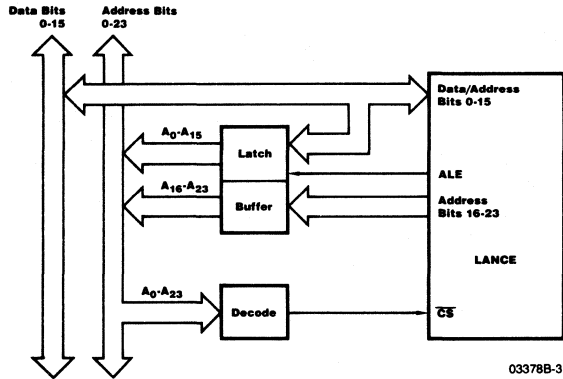
## MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the 68000, Z8000, 8086, and LSI-II devices.

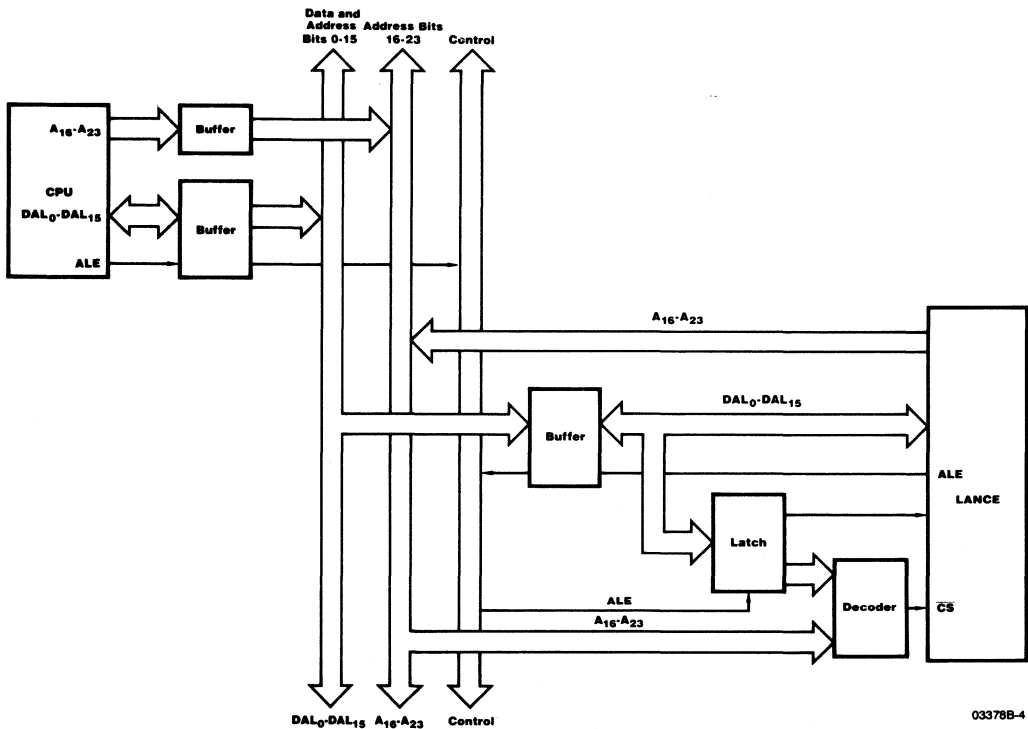
The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. The LANCE interfaces with both multiplexed and demultiplexed data busses (Figure 3), and features control signals for address/data bus transceivers.

Figure 3.

### a) Demultiplexed Bus



### b) Multiplexed Bus System Overview



# Am7960

Coded Data Transceiver

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Universal Networking Transceiver
- High-impedance interface to coupling transformer
  - User-transparent Manchester encoding/decoding
  - Glitch-free power up/down
- "Modem-like" controller interface
- 32 dB dynamic range (transmit to receive)
- Transmit edge rate control
- Up to 3 Mbps data rate

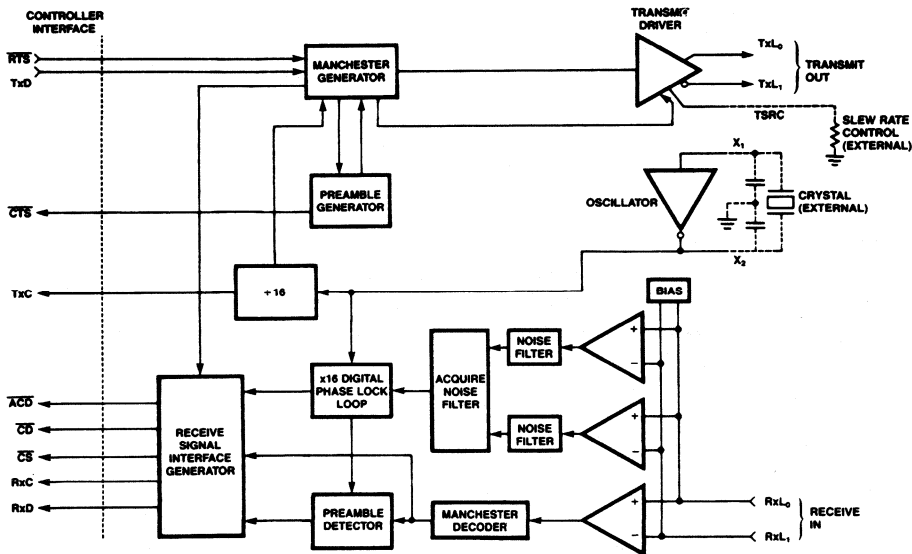
## GENERAL DESCRIPTION

The Am7960 is a combined Manchester encoder/decoder and transceiver. It is designed for use in synchronous communications systems which require common mode isolation in point-to-point or common bus architecture, supporting data rates of up to 3 Mbps. This 5-V device provides 32 dB of dynamic range, and guarantees 2-V output into 37.5  $\Omega$ . A single external component controls the slew rate of the transmitter, and a signal qualifier in the receiver minimizes false starts, improving reliability.

The Am7960 has a modem-like controller interface which makes it compatible with nearly every existing synchronous communications controller (USARTs, SCCs, etc).

The use of ECL circuitry to process signals internal to the Am7960 chip enhances device speed. I/O pins operate at TTL/MOS logic levels to allow convenient interfacing with other devices such as the AmZ8530\* Serial Communications Controller.

## BLOCK DIAGRAM



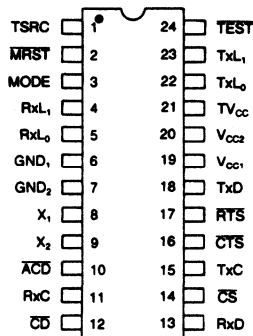
BD005440

## RELATED AMD PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet
Am7992B	Serial Interface Adapter
Am7995	Ethernet Transceiver
AmZ8530	Serial Communications Controller

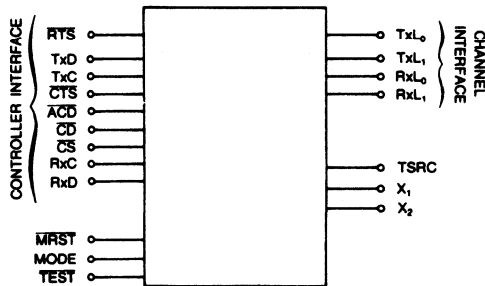
\*Z8530 is a trademark of Zilog, Inc.

## CONNECTION DIAGRAM



CD007050

## LOGIC SYMBOL

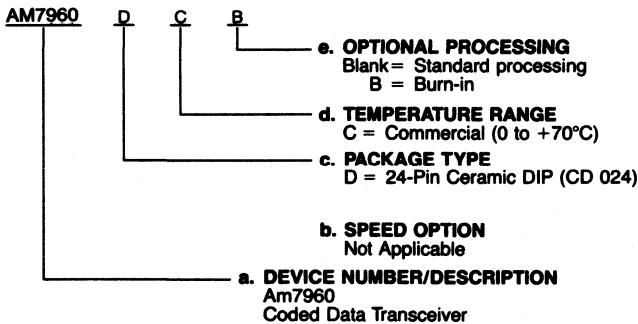


LS001950

## ORDERING INFORMATION Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7960	DC, DCB

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am7990

Local Area Network Controller for Ethernet (LANCE)

## DISTINCTIVE CHARACTERISTICS

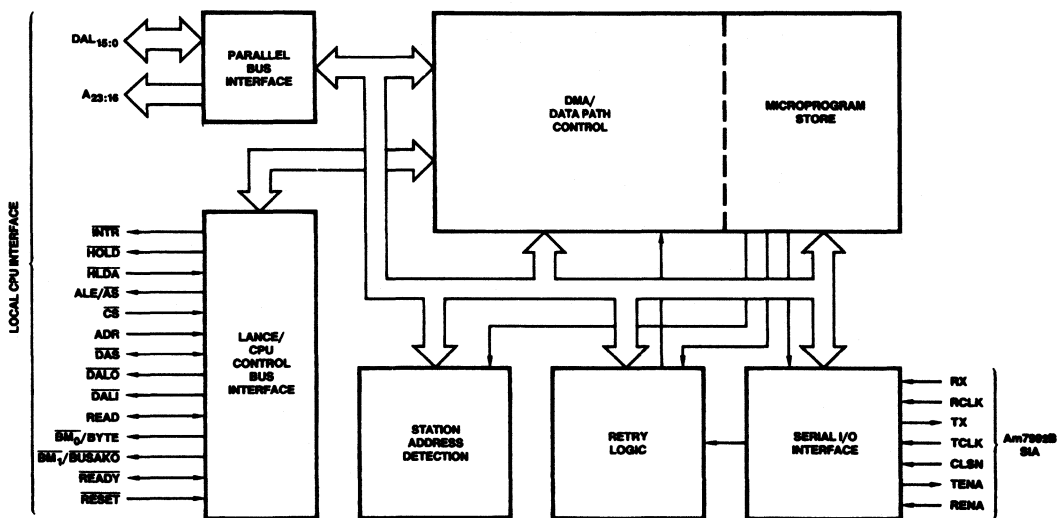
- Compatible with Ethernet and IEEE-802.3 (10Base5 Type A, and 10Base2 Type B, "Cheapernet")
- Easily interfaced to 8086, 68000, Z8000\*, LSI-II\*\* microprocessors
- On-board DMA and buffer management, 48 byte FIFO
- 24-bit wide linear addressing (Bus Master Mode)
- Network and packet error reporting
- Back-to-back packet reception with as little as 4.1  $\mu$ sec interpacket gap time
- Diagnostic routines
  - Internal/external loop back
  - CRC logic check
  - Time domain reflectometer

## GENERAL DESCRIPTION

The Am7990 Local Area Network Controller for Ethernet (LANCE) is a 48-pin VLSI device designed to greatly simplify interfacing a microcomputer or minicomputer to an IEEE-802.3/Ethernet Local Area Network. The LANCE, in conjunction with the Am7992B Serial Interface Adapter (SIA), Am7996 Transceiver, and closely coupled local memory and microprocessor, is intended to provide the user

with a complete interface module for an Ethernet network. The Am7990 is designed using a scaled N-Channel MOS technology, and is compatible with a variety of microprocessors. On-board DMA, advanced buffer management, and extensive error reporting and diagnostics facilitate design and improve system performance.

## BLOCK DIAGRAM



BD002063

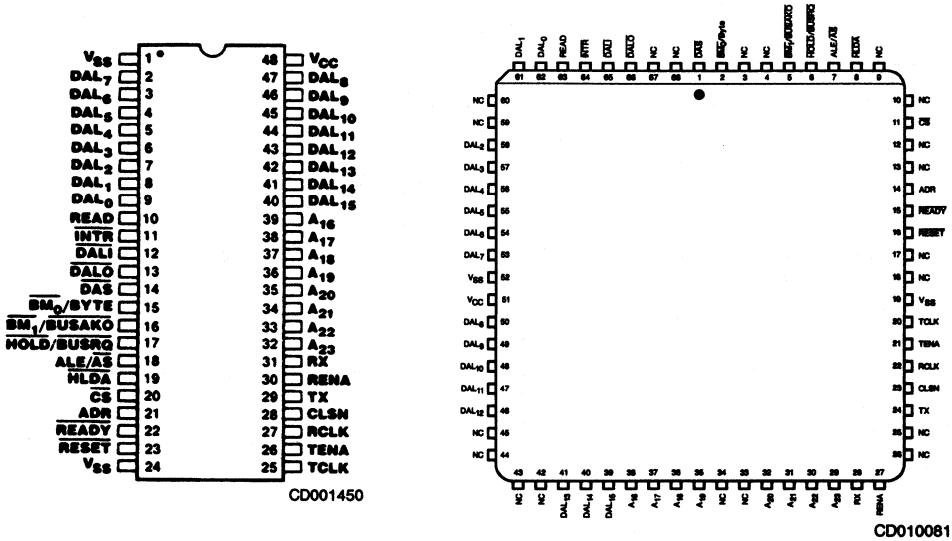
## RELATED AMD PRODUCTS

Part No.	Description
Am7992B	Serial Interface Adaptor (SIA)
Am7996	IEEE-802.3/Ethernet/Cheapernet Transceiver

\*Z8000 is a trademark of Zilog, Inc.

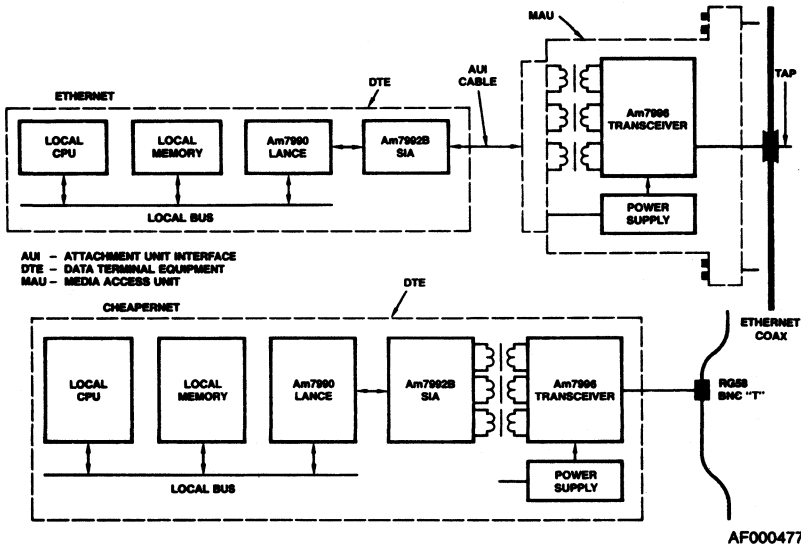
\*\*LSI-II is a registered trademark of Digital Equipment Corporation.

## CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

## TYPICAL ETHERNET/CHEAPERNET NODE



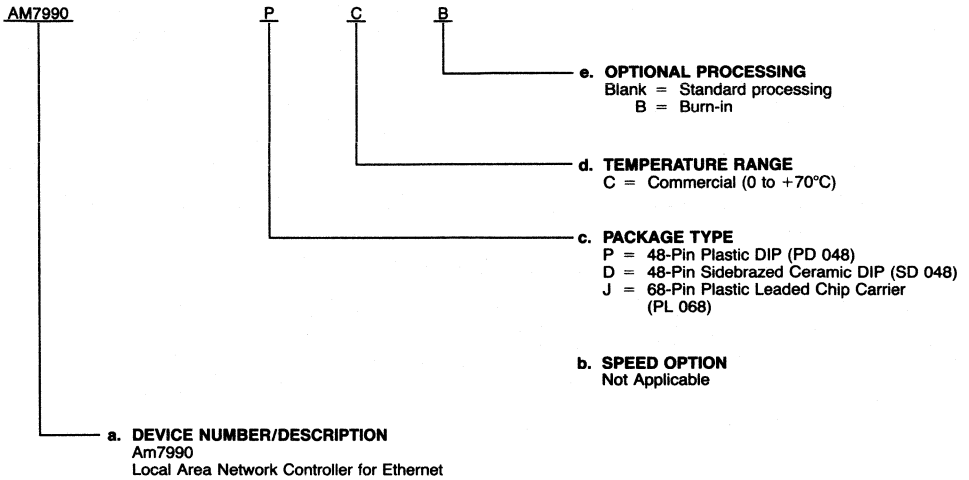


# ORDERING INFORMATION

## Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7990	DC, DCB, PC, PCB, JC, JCB

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Am7992B

Serial Interface Adapter (SIA)

## DISTINCTIVE CHARACTERISTICS

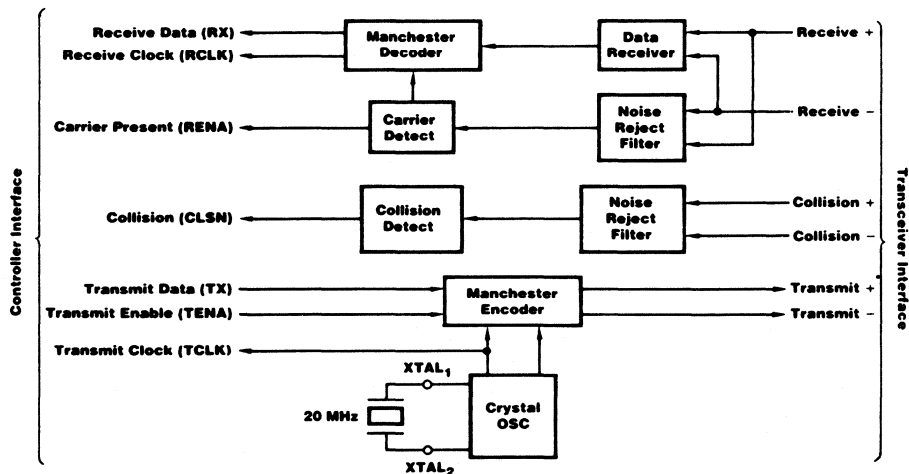
- Compatible with Ethernet/Cheapernet/IEEE-802.3 specifications
- Crystal-controlled Manchester Encoder
- Manchester Decoder acquires clock and data within four bit times with an accuracy of  $\pm 3$  ns
- Guaranteed carrier and collision detection squelch threshold limits
  - Carrier/collision detected for inputs greater than  $-275$  mV
  - No carrier/collision for inputs less than  $-175$  mV
- Input signal conditioning rejects transient noise
  - Transients  $< 10$  ns for collision detector inputs
  - Transients  $< 20$  ns for carrier detector inputs
- Receiver decodes Manchester data with worst-case  $\pm 19$  ns of clock jitter (at 10 MHz)
- TTL-compatible host interface
- Transmit accuracy  $\pm 0.01\%$  (without adjustments)

## GENERAL DESCRIPTION

The Am7992B Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with IEEE-802.3, Cheapernet and Ethernet specifications. In an IEEE-802.3/Ethernet application, the Am7992B interfaces the Am7990 Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable, acquires clock

and data within four bit times, and decodes Manchester data with worst-case  $\pm 19$  ns phase jitter at 10 MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

## BLOCK DIAGRAM

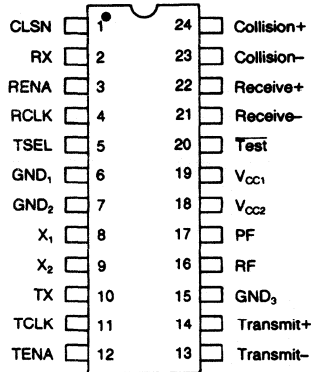


BD002071

## RELATED AMD PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE-802.3/Ethernet/Cheapernet Transceiver

## CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation

CD001521

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM7992B

P

C

B

**e. OPTIONAL PROCESSING**

Blank = Standard processing  
B = Burn-in

**d. TEMPERATURE RANGE**

C = Commercial (0 to +70°C)

**c. PACKAGE TYPE**

P = 24-Pin Slim Plastic DIP (PD 3024)  
D = 24-Pin Slim Ceramic DIP (CD3024)

**b. SPEED OPTION**  
Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**

Am7992B  
Serial Interface Adapter

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM7992B	PC, PCB, DC, DCB

# Am7996

IEEE-802.3/Ethernet/Cheapernet Transceiver

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet Version 2 and IEEE-802.3 10Base5 (Type A) and 10Base2 (Type B) specifications
- Pin-selectable SQE Test (Heartbeat) option
- Internal Jabber Controller prevents excessive transmission time
- Noise rejection filter ensures only valid data is transmitted onto network
- Collision detection on both transmit and receive data
- Collision detect threshold levels adjustable for other networking applications

## GENERAL DESCRIPTION

The Am7996 IEEE-802.3/Ethernet/Cheapernet Transceiver supports Ethernet Version 2, IEEE-802.3 (Type A), and IEEE-802.3 (Type B - Cheapernet) transceiver applications. Transmit, receive, and collision detect functions at the coaxial media interface to the Data Terminal Equipment (DTE) are all performed by this single device.

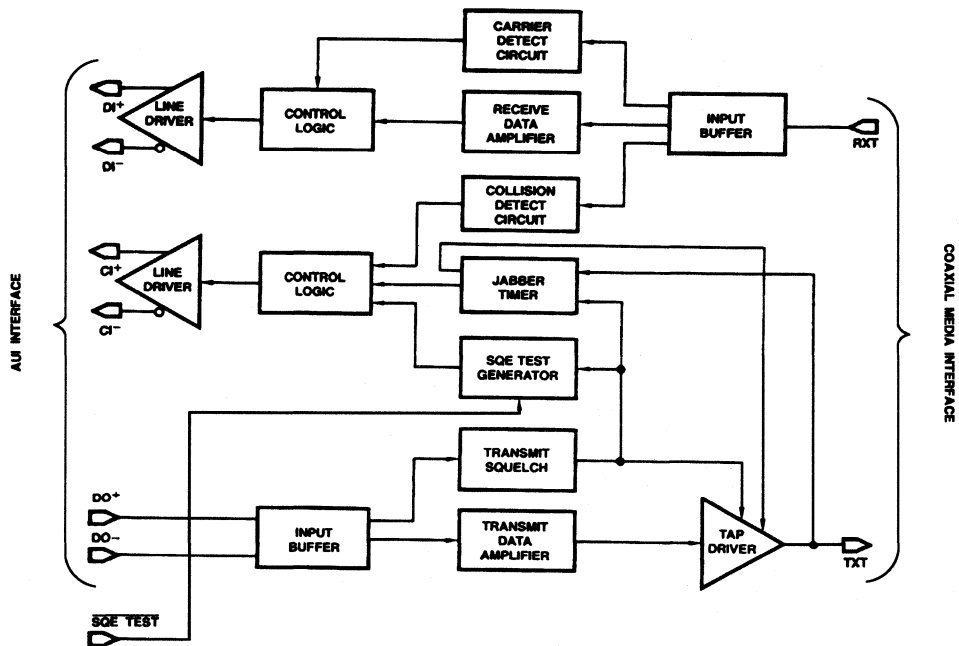
In an IEEE-802.3 (Type A)/Ethernet application, the Am7996 interfaces the coaxial (0.4" diameter) media to the DTE through an isolating pulse transformer and the 78- $\Omega$  Attachment Unit Interface (AUI) cable. In IEEE-802.3 Type B - Cheapernet applications, the Am7996 typically resides inside the DTE with its signals to the DTE isolated and the coaxial (0.2" diameter) media directly connected to the

DTE. Transceiver power and ground in both applications are isolated from that of the DTE.

The Am7996's Tap Driver provides controlled skew and current drive for data signalling onto the media. The Jabber Controller prevents the node from transmitting excessively. While transmitting, collisions on the media are detected if one or more additional stations are transmitting.

The Am7996 features an optional SQE Test function that provides a signal on the *CI* pair at the end of every transmission. The SQE Test indicates the operational status of the *CI* pair to the DTE. It can also serve as an acknowledgement to the node that packet transmission onto the coax was completed.

## BLOCK DIAGRAM

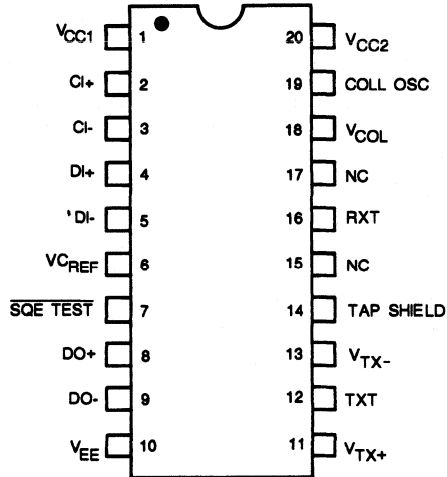


BD005820

## RELATED AMD PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter (SIA)

## CONNECTION DIAGRAM



CD009070

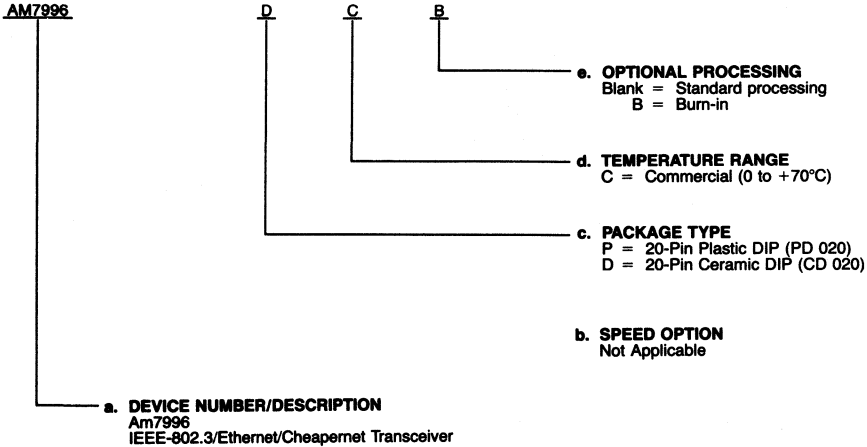
Note: Pin 1 is marked for orientation.  
NC = No Connection

# ORDERING INFORMATION

## Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7996	PC, PCB, DC, DCB

### Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

# **COMMUNICATION PROCESSORS**

# Am7971

## Compression Expansion Processor (CEP with image bit-boundary processing) PRELIMINARY

### DISTINCTIVE CHARACTERISTICS

- Image preserving compression and expansion of two-tone image using run-length (one-dimensional) coding and relative element address (two-dimensional) coding.
- Compatible with internationally accepted CCITT Group III and IV (Recommendations T.4 and T.6) image compression standards.
- Image bit-boundary operations.
- High performance of 1 to 12 MHz pixel rates with 3, 5, and 8MHz clock.
- CPU bus and optional local Document Store Bus with on-chip DMA. The CEP can address up to 16Mbytes on each bus.
- Handles four memory buffers: source and destination buffers for both the compressor and expander.
- Full duplex mode for simultaneous compressor and expander operations with each processor independently programmable.
- On-chip error detection to catch all possible data corruptions and support for easy error recovery.
- 46 user programmable registers allow for very easy and highly flexible system implementation. Includes:
  - Programmable page width (upto 16K pels), frame width and top, left and right margins.
  - Optional Express mode during compression and Granularity mode during expansion for vertical resolution conversion.
  - Programmable K parameter.
  - Optional Wraparound mode.
  - Transparent mode.

### GENERAL DESCRIPTION

The Am7971 Compression Expansion Processor (CEP) with Image Bit-Boundary Processing capacity is a high performance peripheral which compresses and expands two-tone bit mapped images or documents in accordance with internationally accepted CCITT standards. These fully image preserving algorithms reduce storage requirements and data transmission time for systems handling bit-mapped data.

The Am7971 performs one-dimensional Modified Hoffman (MH) run-length coding as well as two-dimensional Modified READ (MR/MMR) relative coding as specified in CCITT Recommendations T.4 and T.6 for Group III and Group IV compatible equipments. The typical compression ratio for the eight CCITT test documents is 5:1 to 50:1.

The compressor and expander operate not only in full duplex mode but each processor can be independently programmed for one-dimensional encoding/decoding, two-dimensional encoding/decoding, or transparent data transfer.

Equipped with an on-chip error detection mechanism, the Am7971 detects all possible data corruptions by checking for illegal codes, negative run-lengths and incorrect line lengths. Furthermore, its architecture allows for error recovery with minimal CPU intervention.

With 46 user programmable registers, standard Am8088-like microprocessor bus interface, dual bus architecture

and on-chip DMA the Am7971 offers tremendous system flexibility and ease of implementation. After initialization the Am7971 will operate with minimal CPU overhead. Its status is available through polled registers and exception conditions may be signalled using an external interrupt.

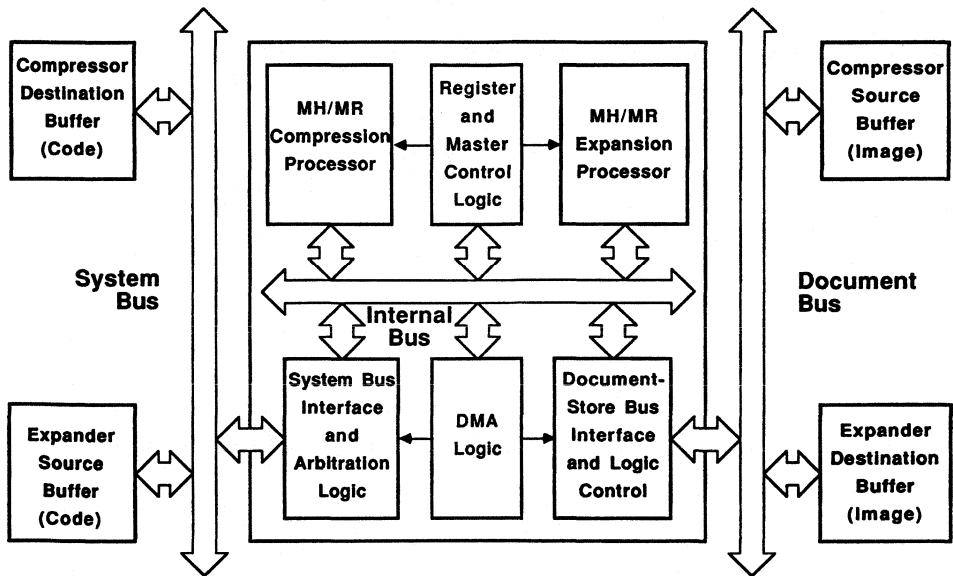
Document page width is programmable upto 16K picture elements (pels). Programmable frame width enable windowing features and programmable top, left and right margins allow image boundaries to be left blank.

Optional express mode allows one line to be skipped after every 'nth' line to accelerate compression ( $n = 1$  to 255). On the expansion side, the granularity option allows the processor to duplicate every mth line ( $m = 1$  to 7).

In two-dimensional mode, the programmable K-parameter ( $k = 1$  to 255 and infinity) defines the number of lines to be encoded in 2-D coding sequence before a 1-D line is inserted. For error free environments (Group 4)  $K = \text{infinity}$  allows for maximum compression.

The CEP can address up to 16 Mbytes of memory on each bus and two buffers (source and destination) on both the compressor and expander. Starting address, buffer length and current address for image and coded data are stored in internal registers independently for both the compressor and expander.



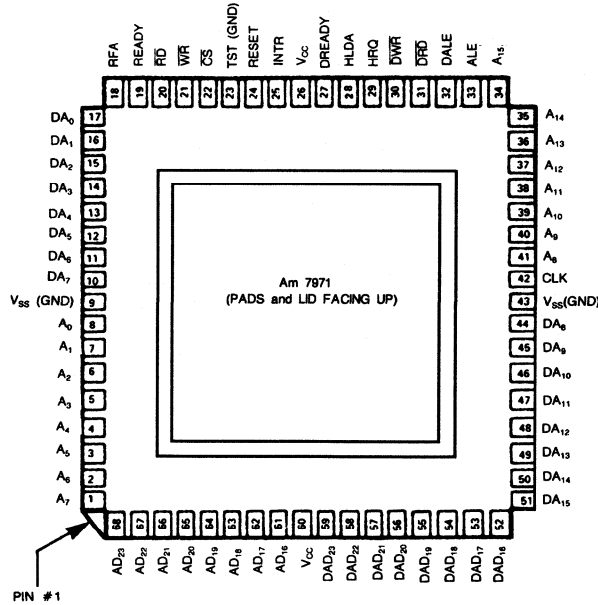


TB000410

**Figure 1. Am7971 Block Diagram**

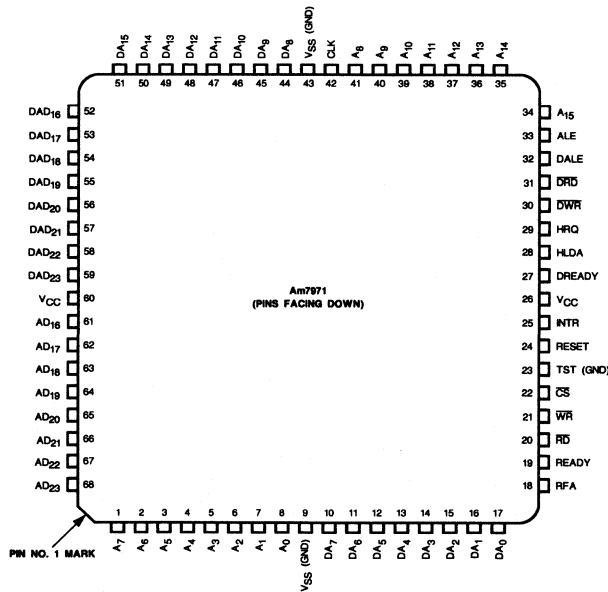
RELATED AMD PRODUCTS	
Part No.	Description
Am7971 EVAL	Am7971 Evaluation Board

# CONNECTION DIAGRAMS



CD010341

Figure 2. Am7971 Pin Out for Leadless Chip Carrier (LCC)



CD010331

Figure 3. Am7971 Pin Out for Plastic Leaded Chip Carrier (PLCC)

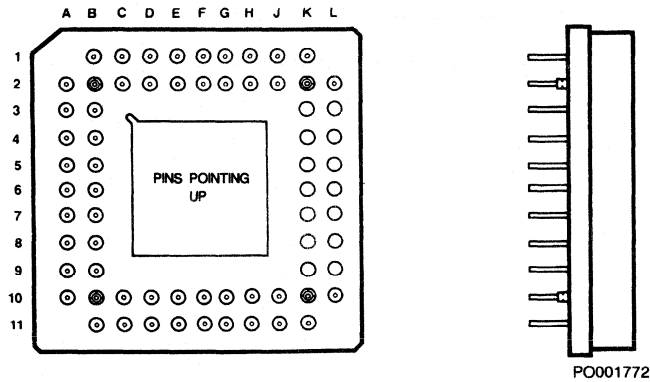


Figure 4. Am7971 (CEP) Pin Out for a Pin Grid Array (PGA) Package

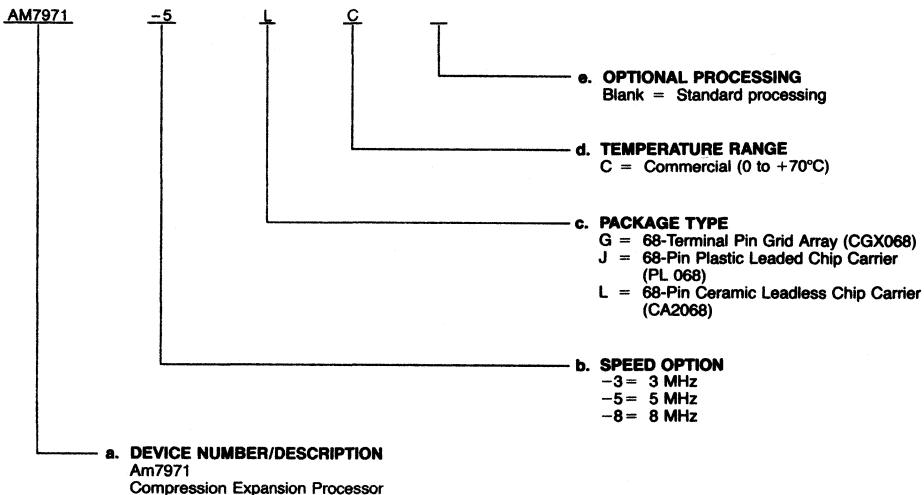
PIN DESIGNATIONS							
(SORTED BY PIN NAME)				(SORTED BY PIN NUMBER)			
PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A <sub>0</sub>	E-2	DA <sub>7</sub>	F-2	A-2	AD <sub>23</sub>	G-1	DA <sub>6</sub>
A <sub>1</sub>	E-1	DA <sub>8</sub>	F-10	A-3	AD <sub>21</sub>	G-2	DA <sub>5</sub>
A <sub>2</sub>	D-2	DA <sub>9</sub>	E-11	A-4	AD <sub>19</sub>	G-10	CLK
A <sub>3</sub>	D-1	DA <sub>10</sub>	E-10	A-5	AD <sub>17</sub>	G-11	A <sub>8</sub>
A <sub>4</sub>	C-2	DA <sub>11</sub>	D-11	A-6	V <sub>CC</sub>	H-1	DA <sub>4</sub>
A <sub>5</sub>	C-1	DA <sub>12</sub>	D-10	A-7	DAD <sub>22</sub>	H-2	DA <sub>3</sub>
A <sub>6</sub>	B-2	DA <sub>13</sub>	C-11	A-8	DAD <sub>20</sub>	H-10	A <sub>9</sub>
A <sub>7</sub>	B-1	DA <sub>14</sub>	C-10	A-9	DAD <sub>18</sub>	H-11	A <sub>10</sub>
A <sub>8</sub>	G-11	DA <sub>15</sub>	B-11	A-10	DAD <sub>16</sub>	J-1	DA <sub>2</sub>
A <sub>9</sub>	H-10	DAD <sub>16</sub>	A-10	B-1	A <sub>7</sub>	J-2	DA <sub>1</sub>
A <sub>10</sub>	H-11	DAD <sub>17</sub>	B-10	B-2	A <sub>6</sub>	J-10	A <sub>11</sub>
A <sub>11</sub>	J-10	DAD <sub>18</sub>	A-9	B-3	AD <sub>22</sub>	J-11	A <sub>12</sub>
A <sub>12</sub>	J-11	DAD <sub>19</sub>	B-9	B-4	AD <sub>20</sub>	K-1	DA <sub>0</sub>
A <sub>13</sub>	K-10	DAD <sub>20</sub>	A-8	B-5	AD <sub>18</sub>	K-2	READY
A <sub>14</sub>	K-11	DAD <sub>21</sub>	B-8	B-6	AD <sub>16</sub>	K-3	WR
A <sub>15</sub>	L-10	DAD <sub>22</sub>	A-7	B-7	DAD <sub>23</sub>	K-4	TST (GND)
AD <sub>16</sub>	B-6	DAD <sub>23</sub>	B-7	B-8	DAD <sub>21</sub>	K-5	INTR
AD <sub>17</sub>	A-5	DALE	L-9	B-9	DAD <sub>19</sub>	K-6	DREADY
AD <sub>18</sub>	B-5	DRD	K-8	B-10	DAD <sub>17</sub>	K-7	HRQ
AD <sub>19</sub>	A-4	DREADY	K-6	B-11	DA <sub>15</sub>	K-8	DRD
AD <sub>20</sub>	B-4	DWR	L-8	C-1	A <sub>5</sub>	K-9	ALE
AD <sub>21</sub>	A-3	HLDA	L-7	C-2	A <sub>4</sub>	K-10	A <sub>13</sub>
AD <sub>22</sub>	B-3	HRQ	K-7	C-10	DA <sub>14</sub>	K-11	A <sub>14</sub>
AD <sub>23</sub>	A-2	INTR	K-5	C-11	DA <sub>13</sub>	L-2	RFA
ALE	K-9	RD	L-3	D-1	A <sub>3</sub>	L-3	RD
CLK	G-10	READY	K-2	D-2	A <sub>2</sub>	L-4	CS
CS	L-4	RESET	L-5	D-10	DA <sub>12</sub>	L-5	RESET
DA <sub>0</sub>	K-1	RFA	L-2	D-11	DA <sub>11</sub>	L-6	V <sub>CC</sub>
DA <sub>1</sub>	J-2	TST (GND)	K-4	E-1	A <sub>1</sub>	L-7	HLDA
DA <sub>2</sub>	J-1	V <sub>CC</sub>	A-6	E-2	A <sub>0</sub>	L-8	DWR
DA <sub>3</sub>	H-2	V <sub>CC</sub>	L-6	E-10	DA <sub>10</sub>	L-9	DALE
DA <sub>4</sub>	H-1	V <sub>SS</sub> (GND)	F-1	E-11	DA <sub>9</sub>	L-10	A <sub>15</sub>
DA <sub>5</sub>	G-2	V <sub>SS</sub> (GND)	F-11	F-1	V <sub>SS</sub>		
DA <sub>6</sub>	G-1	WR	K-3	F-2	DA <sub>7</sub>		
				F-10	DA <sub>8</sub>		
				F-11	V <sub>SS</sub>		

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM7971-3	JC
AM7971-5	GC, JC, LC
AM7971-8	GC, LC

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# Z8030/Z8530

## Serial Communications Controller

### DISTINCTIVE CHARACTERISTICS

- Two 1 Mbps full-duplex serial channels
  - Each channel has independent oscillator, baud-rate generator, and PLL for clock recovery
- Programmable protocols:
  - NRZ, NRZ1, and FM data encoding
- Programmable Asynchronous Modes
  - 5- to 8-bit characters with programmable stop bits, clock, break detect, and error conditions
- Programmable Synchronous Modes
  - SDLC and HDLC, and SDLC loop supported with frame control, zero insertion and deletion, abort, and residue handling
  - CRC-16 and CCITT generators and checkers
- Z8000\* compatible
  - The Z8030 interfaces directly with the Z8000 CPU bus and to the Z8000 interrupt structure
- Compatible with non-multiplexed bus
  - The Z8530 interfaces easily to most other CPUs

### GENERAL DESCRIPTION

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats; synchronous byte-oriented protocols, such as IBM Bisync; and synchronous bit-oriented protocols, such as HDLC and IBM SDLC.

This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

The device can generate and check CRC codes in any synchronous mode, and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The SCC is offered in two versions. The Z8030 is directly compatible with the Z8000 and 8086 CPUs. The Z8530 is designed for non-multiplexed buses and is easily interfaced with most other CPUs, such as 8080, Z80, 6800, 68000, and †Multibus.

### BLOCK DIAGRAM

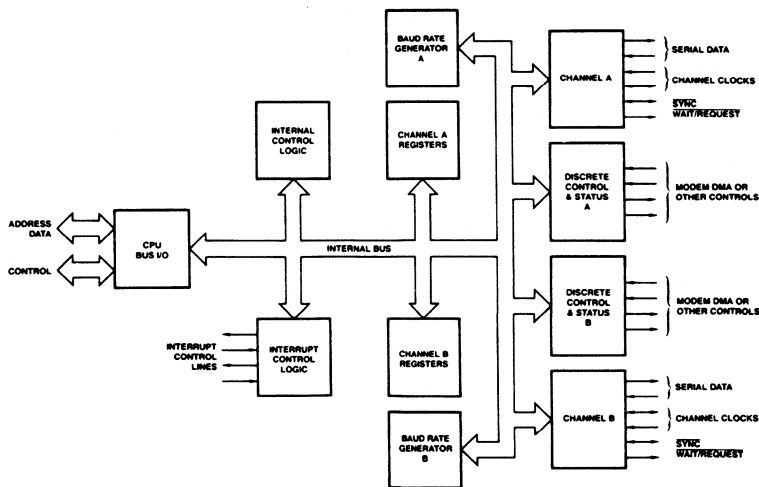


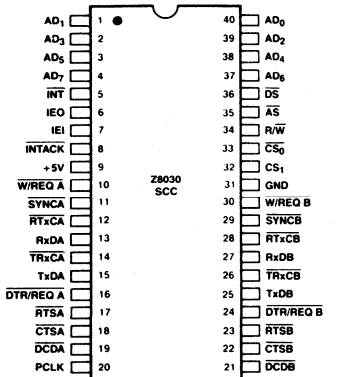
Figure 1.

BD003520

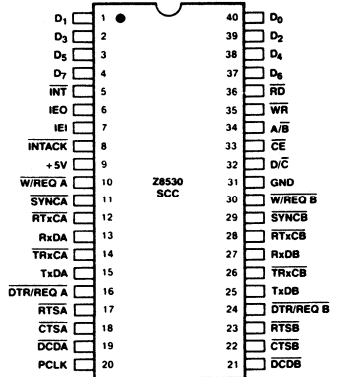
### RELATED AMD PRODUCTS

See the [Z8030/Z8530 Serial Communications Controller Technical Manual](#) - 1987 edition (07513B) for detailed technical information.

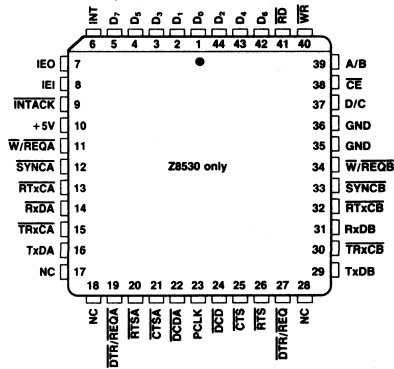
## CONNECTION DIAGRAMS



CD005350



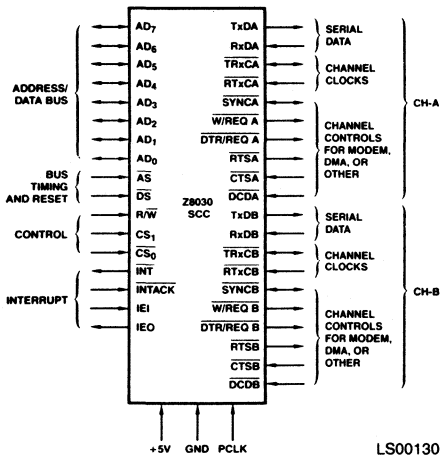
CD005360



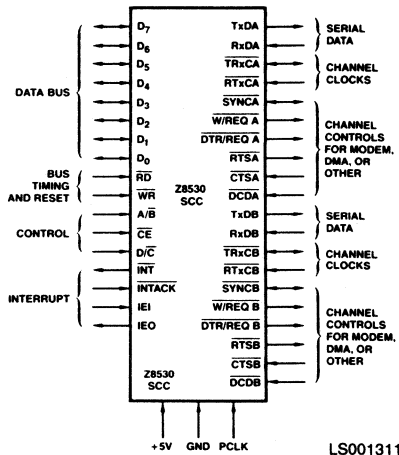
NC = No Connection  
GND = Ground

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL



LS001300



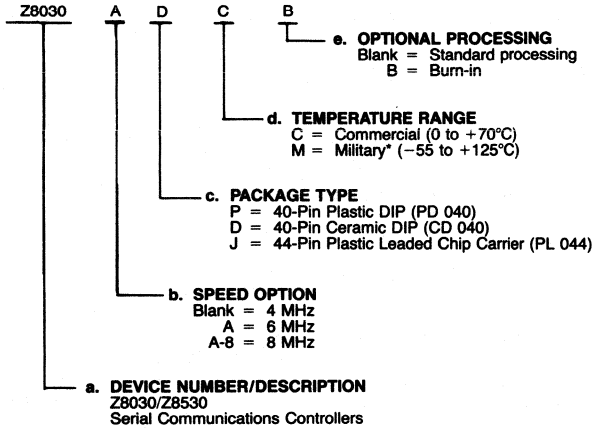
LS001311

## ORDERING INFORMATION

### Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
Z8030	PC, DC, DCB
Z8030A	
Z8530	PC, DC, DCB, DMB, JC
Z8530A	
Z8530A-8	PC, DC, DCB, JCB

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

\* Military temperature range products are NPL (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

# Am9518/AmZ8068

## Data Ciphering Processor

### DISTINCTIVE CHARACTERISTICS

- Encrypts and decrypts data
  - Implements National Bureau of Standards standard data encryption algorithm.
- High-Speed Operation
  - Am9518 and AmZ8068 throughput over 1.3 and 1.7M bytes per second, respectively. Operates at data rates fast enough for disk controllers, high-speed DMA, telecommunication channels.
- Supports three ciphering options
  - Electronic Code Book for disk applications. Chain Block Cipher for high-speed telecommunications. Cipher Feedback for low-to-medium speed, byte-oriented communications.
- Three separate key registers on-chip
  - Separate registers for encryption key, decryption key and master key improve system security and throughput by eliminating need to reload keys frequently.
- Three separate data ports provide flexible interface, improved security
  - The DCP utilizes a master port, slave port and key port. Functions of the three ports can be programmed by the user to provide for simple interface to AmZ8000 and Am2900 systems and to provide total hardware separation of encrypted data, clear data and keys.

### GENERAL DESCRIPTION

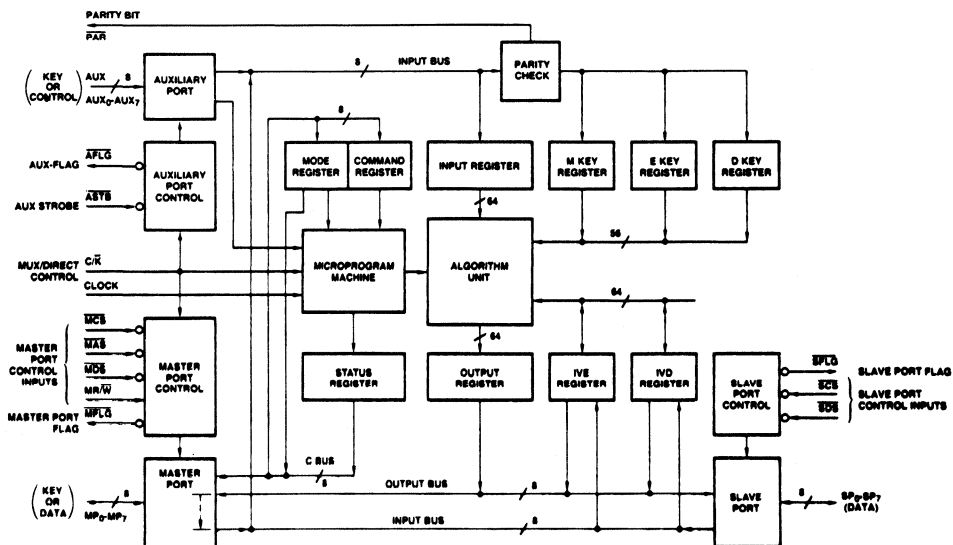
The Am9518/AmZ8068 Data Ciphering Processor is an N-channel silicon gate LSI product containing the circuitry necessary to encrypt and decrypt data using the National Bureau of Standards encryption algorithm. It is designed to be used in a variety of environments, including dedicated controllers, communication concentrators, terminals, and peripheral task processors in general processor systems.

The DCP provides a high throughput rate using Cipher Feedback, Electronic Code Book, or Cipher Block Chain operating modes. Separate ports for key input, clear data, and enciphered data enhance security.

The system communicates with the DCP using commands entered in the master port and through auxiliary control lines. Once set up, data can flow through the DCP at high speeds because input, output, and ciphering activities are all performed concurrently. External DMA control can easily be used to enhance throughput in some system configurations.

This device is designed to interface directly to the AmZ8000 CPU bus and, with a minimum of external logic, to the 2900, MC68000, 8086, 8085, and 8051 families of processors.

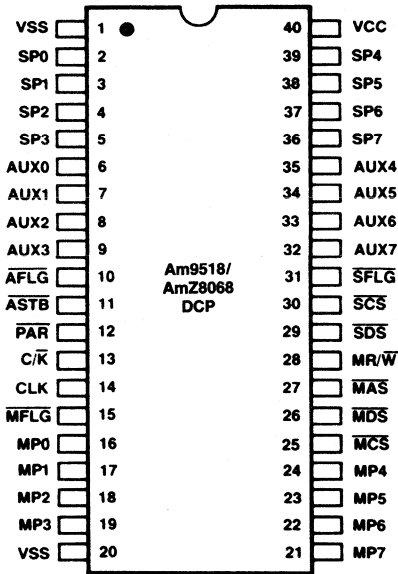
### BLOCK DIAGRAM



BD003290



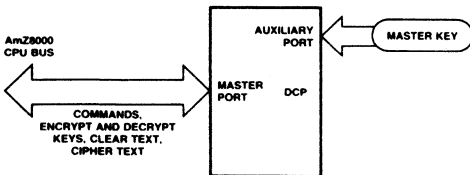
# CONNECTION DIAGRAM



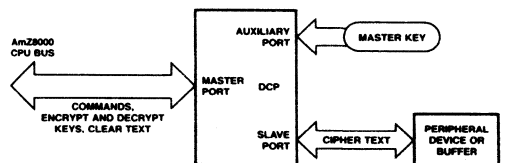
CD005111

Note: Pin 1 is marked for orientation

## DCP DATA FLOW OPTIONS



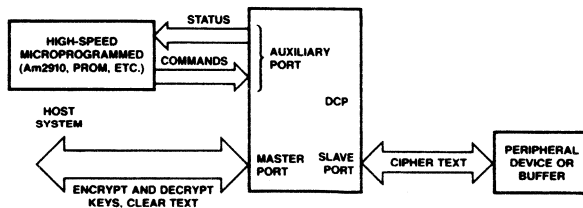
AF002220



AF002230

## Single-Port Configuration, Multiplexed Control

## Dual-Port Configuration, Multiplexed Control



AF002240

## Dual-Port Configuration, Direct Control



# **TELECOMMUNICATIONS SUPPORT TOOLS**

## **MODEM EVALUATION SYSTEM**

### **Am79C12/79CV12 Modem Evaluation Board**

The Am79C12/79CV12 Modem Evaluation Board provides a ready-made environment to evaluate and exercise the Am79C12/Am79CV12 Full-Duplex 1200/300 bps Modem from both a hardware and software perspective. The dual-mode board is designed either to fit in a vacant slot of an IBM-PC or compatible unit, or to serve as a stand-alone tool in a non-PC environment. The PC Mode, window-driven software allows extensive control over the Am79C12/79CV12 Modem, featuring automatic dialing and answering functions. In the Stand-alone Mode, an on-board Am8031 Microcontroller (with external EPROM) interprets commands received via its serial interface from an RS-232C terminal. The on-board Data Access Arrangement provides a convenient and protective interface to the telephone network.

### **Hayes AT update option**

The Am79C12/79CV12 Modem Evaluation Board equipped with the "Hayes EPROM" provides a ready-made demonstration of Hayes compatibility using the Am79C12/79CV12 Full-Duplex 1200/300 bps Modem. The board, designed to stand alone as a Hayes Compatible "Box" Modem, allows an extensive evaluation of the industry-standard 'AT' Command Set. An on-board Am8031 Microcontroller (with external EPROM) interprets 'AT' Commands received via its serial interface from an RS-232C terminal. The on-board Data Access Arrangement provides a convenient and protective interface to the telephone network.

### **Am79C12/79CV12 and Am79C13 AT/DEMO Modem Half Card**

The Am79C12/79CV12 and Am79C13 Hayes-Compatible Modem Half Card provides a ready-made demonstration of Hayes compatibility using the Am79C12/79CV12 Full-Duplex 1200/300 bps Modem. The AT/DEMO Board, designed to fit in a vacant slot of an IBM-PC or compatible unit, allows an extensive evaluation of the industry-standard 'AT' Command Set. The on-board Am7913/Am79C13 'AT' Modem Controller with internally masked ROM interprets 'AT' Commands received via its serial interface from the on-board 8250 UART. Optional external EPROM access is included to allow user-customization of code in addition to the 'AT' Command Set within the Am7913/Am79C13 Controller. The on-board Data Access Arrangement provides a convenient and protective interface to the telephone network. A speaker driver circuit allows "hands-free" feedback of the modem tones on the telephone line.

# ISDN EVALUATION SYSTEM

## **Am79B3xx-Series ISDN Evaluation Kits**

The Am79B3xx-Series ISDN Evaluation Kits provide ready-made hardware and software tools to create a system environment where Am79xx-family ISDN components can be programmed, evaluated, and exercised. The Am79B3xx-Series ISDN Evaluation Kits include:

**Am79B300 Kit:** Am79B300-1 DSC Evaluation Board  
Am79B300-3 DSC Evaluation Software  
Am79B300-4 DSC Evaluation Board Manual  
Am79B300-5 DSC Evaluation Procedures

**Am79B310 Kit:** Am79B310-1 DEC Evaluation Board  
Am79B310-2 DEC Connector Board with ribbon cable  
Am79B310-3 DEC Evaluation Software  
Am79B310-4 DEC Evaluation Board Manual  
Am79B310-5 DEC Evaluation Procedures

## **Am79B300 DSC Evaluation Board**

The Am79B300-1 DSC Evaluation Board provides a ready-made environment to evaluate and exercise either the Am79C30 Digital Subscriber Controller or the Am79C32 ISDN Data Controller from both a hardware and software perspective. The board, designed to fit in a vacant card slot of an IBM-PC or compatible unit, offers the PC backplane or PC co-processor board easy access to the 'S' interface through the Am79C30 DSC. The included menu-driven software allows extensive control over the Am79C30 DSC and its auxiliary hardware. A set of connectors provides convenient access to the Audio and Serial ports of the Am79C30 DSC as well as the 'S' interface.

## **Am79B310 DEC Evaluation Board**

The Am79B310-1 DEC Evaluation Board, and its companion Am79B310-2 Connector Board, provide a ready-made environment to evaluate and exercise the Am79C31 Digital Exchange Controller or Am79C312 Digital Transceiver Controller, and the Am7901A Subscriber Line Audio-Processing Circuit from both a hardware and software perspective. The board, designed for placement in a vacant card slot of an IBM-PC or compatible unit, offers the PC backplane or PC co-processor board easy access to the 'S' interface through the Am79C31 DEC. The included menu-driven software allows extensive control over the Am79C31 DEC and its auxiliary hardware. The Am79B310-2 Connector Board allows convenient access to the dual PCM highways of the Am79C30 and Am7901A.

# VOICE SWITCHING EVALUATION SYSTEM

## **SLC-0xB-Series SLIC/SLAC Evaluation Boards**

AMD's SLC-0xB-Series SLIC/SLAC Evaluation Boards provide ready-made hardware tools to create either a linecard environment or a stand-alone test fixture for the Am79xx family of SLIC/SLAC devices. The SLC-0xB-Series SLIC/SLAC Evaluation Boards include:

- SLC-01B SLIC Evaluation Board
- SLC-03B Low Noise SLAC Evaluation Board
- SLC-08B SLAC Programming Board

## **The SLC-01B SLIC Evaluation Board**

The SLC-01B SLIC Evaluation Board provides a ready-made test setup for evaluating the performance of Am795x-Series Subscriber Line Interface Circuits. It supports a 256-kHz on-board clock to activate the switching regulator in the SLIC. The four-wire receive gain, the two-wire terminating impedance and the D.C. feed characteristics can be programmed by connecting appropriate impedances across binding posts fastened to the evaluation board. The four-wire analog interface is presented through BNC connectors. The two-wire port includes a protection circuitry and a means to provide the necessary ring voltage to the subscriber. This board requires a  $-48\text{ V}$  and a  $\pm 5\text{ V}$  power supply.

## **SLC-03B Low Noise SLAC Evaluation Board**

The SLC-03B Low Noise SLAC Evaluation Board provides a ready-made stand-alone test setup for the Am7901 A/B Subscriber Line Audio Processing Circuit. A 2.048-MHz on-board clock generator caters to the timing requirements of the SLAC. A pair of BNC connectors provide convenient access to the analog input and output terminals of the SLAC. The SLAC programming terminals (Din, Dout, Dclk and CS) are wired to banana sockets to provide easy access to a controller (such as SLC-08B). This board requires a  $\pm 5\text{ V}$  power supply.

## **SLC-08B SLAC Programming Card**

The SLC-08B SLAC Programming Board is designed around an 8085 CPU. It consists of a SLAC firmware monitor and a 28-pin socket to house the SLAC. When this board is executing the SLAC monitor program, it accepts SLAC Control Words and DSP Filter Coefficients in Hexadecimal format through its integral keyboard. The SLAC programming board requires a  $\pm 5\text{ V}$  power supply.

# **SLAC COEFFICIENT DEVELOPMENT SOFTWARE: AmSLAC**

## **Meeting Telephone Network Requirements Using the Am7901A/B SLAC for the Am7905A SLAC with the Am7950/53 SLIC or a Transformer-based SLIC**

### **AmSLAC Manual/Abstract**

The line transmission parameters and system specifications for telephone networks vary from country to country throughout the world and even from local to local within a specific country. To design a generic telephony line card to meet such varied requirements, flexible codecs with user-programmable filters are a necessity for a cost-effective solution. The Am7901A/B or Am7905A Subscriber Line Audio-Processing Circuits (SLACs) along with the Am7950/53 Subscriber Line Interface Circuits (SLICs), or a transformer-based SLIC, can provide the required flexibility (and therefore cost-effective solution) when using filter coefficients developed and optimized over a set of performance criterion by the AmSLAC Program.

The level of system performance achieved by the filter coefficients generated by the AmSLAC Program is directly related to the accuracy of the parameters developed by the user for input to the AmSLAC Program itself. The AmSLAC Manual is intended to address AmSLAC Program input parameters. The AmSLAC Program can then, in turn, generate filter coefficients which will produce good performance to system criterion.

Chapter 1 defines the various transmission parameters normally addressed in the design of a telephony line card. Chapter 2 provides a functional description of the Am7901A/B or Am7905A SLACs along with their configuration with, and modeling of, either an Am7950/53 SLIC or a transformer-based SLIC. Chapter 3 explains the use of the AmSLAC Program, the software tool used to generate a set of SLAC filter coefficients. Chapter 4 recommends equipment configurations and procedures for measuring TWO-WIRE and FOUR-WIRE RETURN LOSS, as well as ATTENUATION DISTORTION and INSERTION LOSS. Chapter 5 provides design examples demonstrating the choice of parameters used as input to the AmSLAC Program. Chapter 6 provides hints to improve the performance of coefficients generated by the AmSLAC Program. Chapter 7 provides a conclusion to the material covered in the previous chapters. Appendix A addresses modeling of the Am7901A/B or Am7905A SLACs with either an Am7950/53 SLIC or transformer-based SLIC. Appendix B describes how to convert a network impedance into an equivalent 'S' domain polynomial. Appendix C describes a circuit for holding loop current.

# Notes



# Notes

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